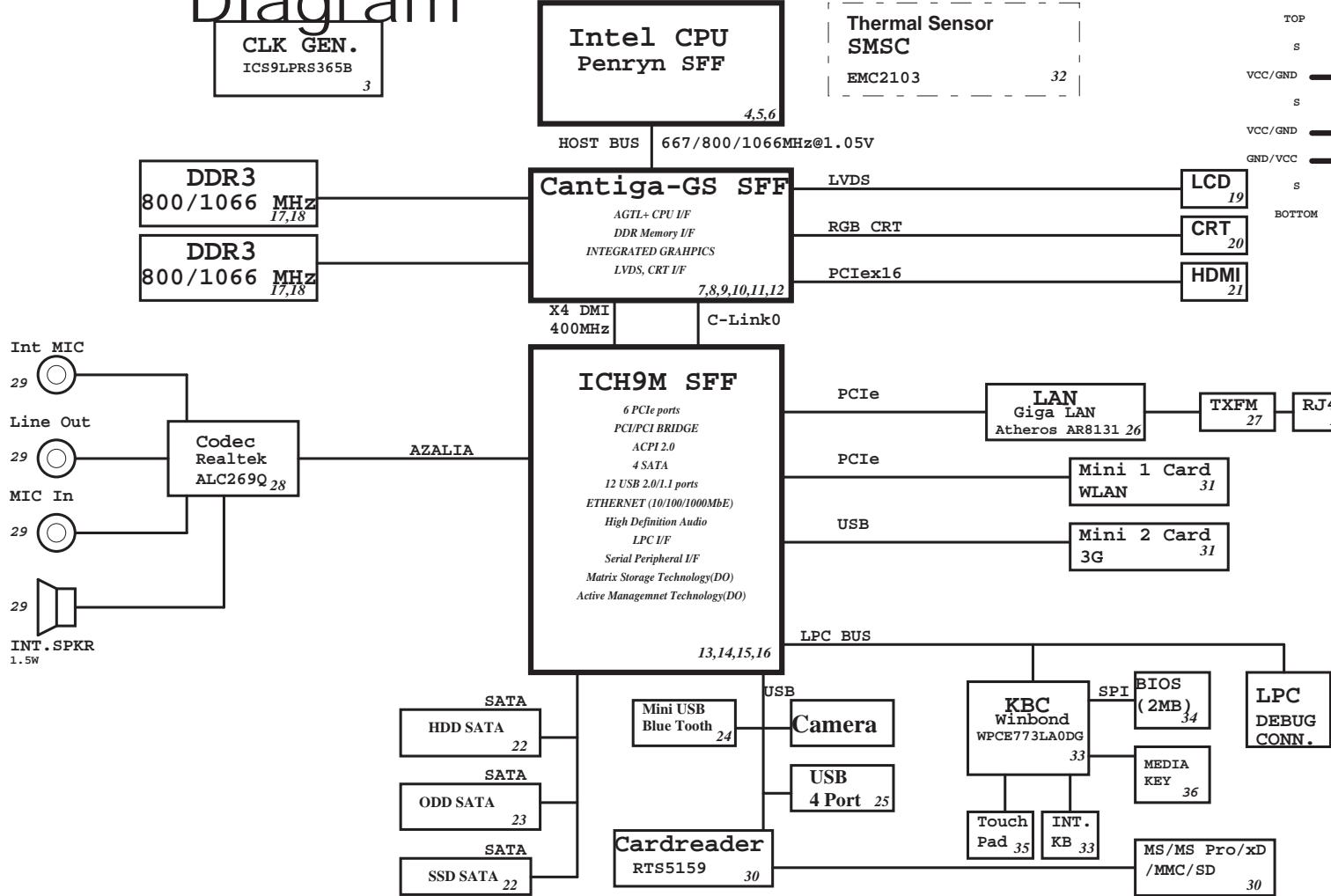


# JM41 Block Diagram



## ICH9M Functional Strap Definitions

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ICH9M Integrated Pull-up  
and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

Cantiga' chipset and ICH9M I/O controller  
Hub strapping configurationMontevina Platform Design guide 22339 0.5  
page 218

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: The Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up  
and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

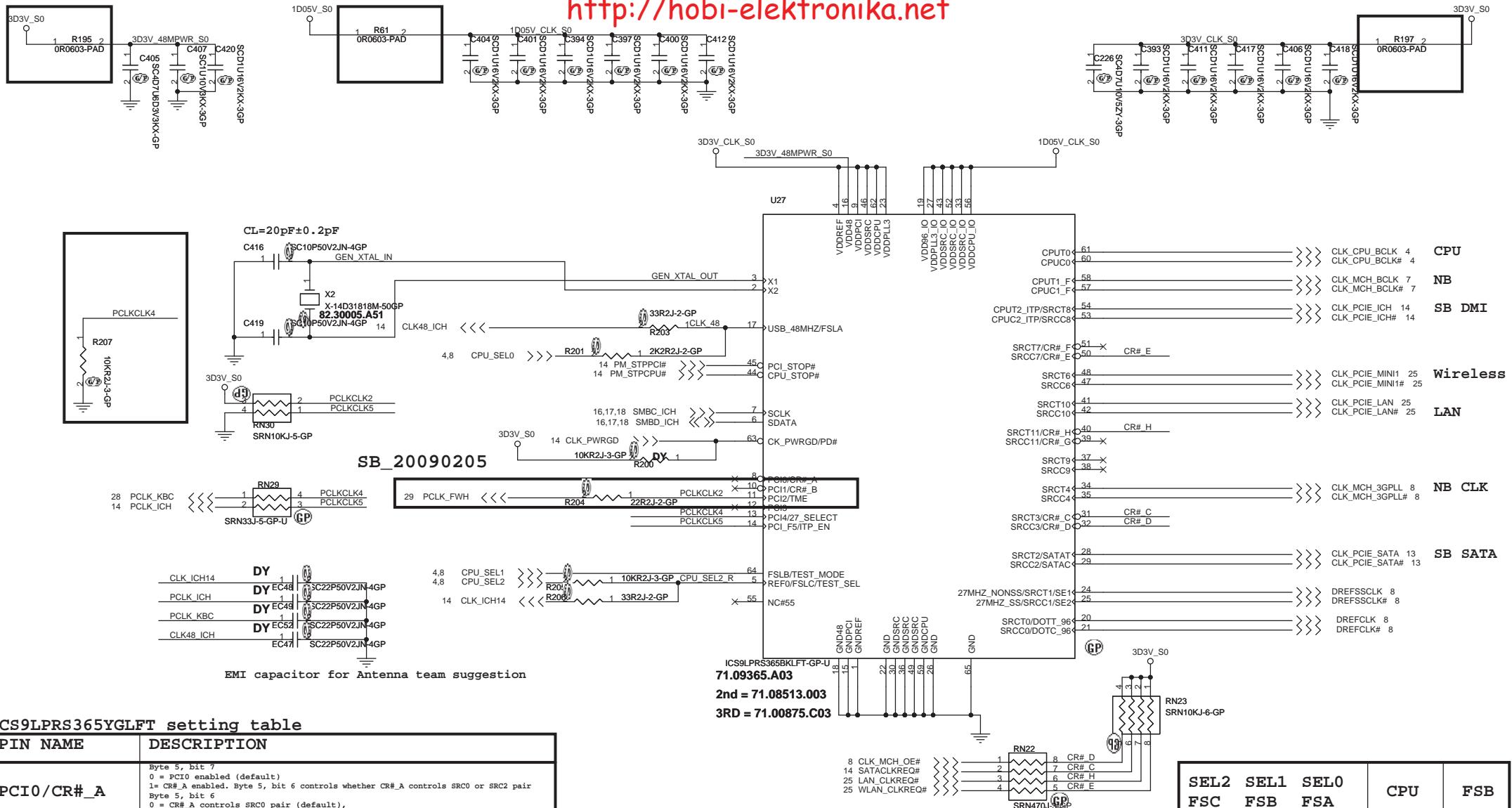
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDO	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG8		
CFG[15:14]		
CFG[18:17]		
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled (Note2) 1= The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1= Normal operation (Default): Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enabled (Note 3) 1= Disabled (default)
CFG13:12	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

## NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

&lt;Core Design&gt;



ICS9LPRS365YGLFT setting table

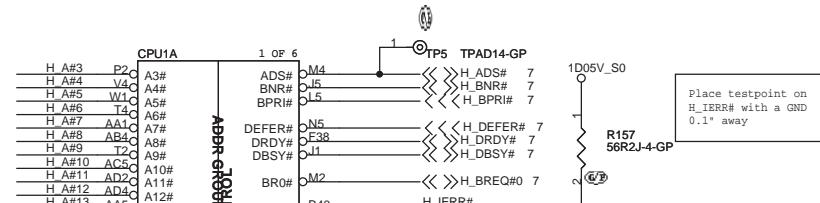
PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1#, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

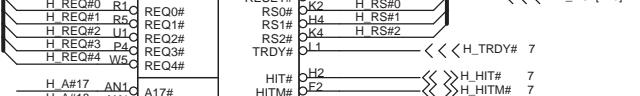
SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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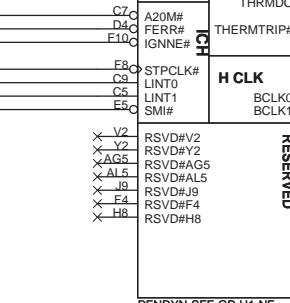
7 H\_A#[35..3] <> H\_A#[35..3]



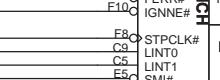
7 H\_ADSTB#0 <> H\_REQ#(4..0)



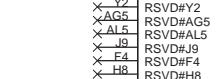
7 H\_ADSTB#1 <> H\_ADSTB1#



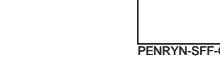
13 H\_A20M# >>>



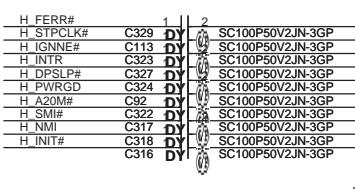
13 H\_FERR# >>>



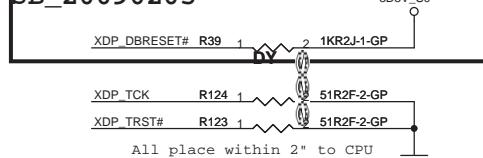
13 H\_STPCLK# >>>



PENRYN-SFF-GP-U1-NF



SB\_20090205



All place within 2" to CPU

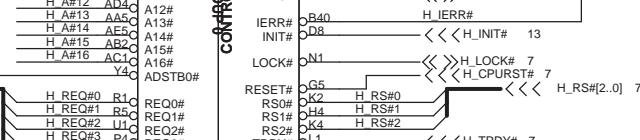
7 H\_DINV#[3..0] <> H\_DINV#[3..0]

H\_DINV#[3..0] <> H\_DINV#[3..0] 7  
H\_DSTBN#[3..0] <> H\_DSTBN#[3..0] 7  
H\_DSTBP#[3..0] <> H\_DSTBP#[3..0] 7  
H\_D#[63..0] <> H\_D#[63..0] 7

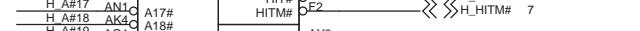
4 H\_BNR# <> H\_BPR#



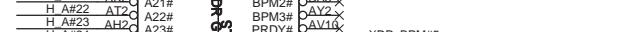
4 H\_DEFER# <> H\_DRDY#



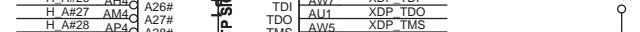
4 H\_BREQ#0 <> H\_IERR#



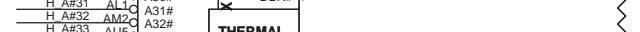
4 H\_IERR# <> H\_INIT#



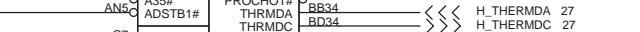
4 H\_LOCK# <> H\_CPURST#



4 H\_RS#0 <> H\_RS#1



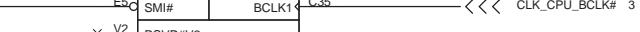
4 H\_RS#1 <> H\_RS#2



4 H\_RS#2 <> H\_RS#3



4 H\_RS#3 <> H\_RS#4



4 H\_RS#4 <> H\_RS#5



4 H\_RS#5 <> H\_RS#6



4 H\_RS#6 <> H\_RS#7



4 H\_RS#7 <> H\_RS#8



4 H\_RS#8 <> H\_RS#9



4 H\_RS#9 <> H\_RS#10



4 H\_RS#10 <> H\_RS#11



4 H\_RS#11 <> H\_RS#12



4 H\_RS#12 <> H\_RS#13



4 H\_RS#13 <> H\_RS#14



4 H\_RS#14 <> H\_RS#15



4 H\_RS#15 <> H\_RS#16



4 H\_RS#16 <> H\_RS#17



4 H\_RS#17 <> H\_RS#18



4 H\_RS#18 <> H\_RS#19



4 H\_RS#19 <> H\_RS#20



4 H\_RS#20 <> H\_RS#21



4 H\_RS#21 <> H\_RS#22



4 H\_RS#22 <> H\_RS#23



4 H\_RS#23 <> H\_RS#24



4 H\_RS#24 <> H\_RS#25



4 H\_RS#25 <> H\_RS#26



4 H\_RS#26 <> H\_RS#27



4 H\_RS#27 <> H\_RS#28



4 H\_RS#28 <> H\_RS#29



4 H\_RS#29 <> H\_RS#30



4 H\_RS#30 <> H\_RS#31



4 H\_RS#31 <> H\_RS#32



4 H\_RS#32 <> H\_RS#33



4 H\_RS#33 <> H\_RS#34



4 H\_RS#34 <> H\_RS#35



4 H\_RS#35 <> H\_RS#36



4 H\_RS#36 <> H\_RS#37



4 H\_RS#37 <> H\_RS#38



4 H\_RS#38 <> H\_RS#39



4 H\_RS#39 <> H\_RS#40



4 H\_RS#40 <> H\_RS#41



4 H\_RS#41 <> H\_RS#42



4 H\_RS#42 <> H\_RS#43



4 H\_RS#43 <> H\_RS#44



4 H\_RS#44 <> H\_RS#45



4 H\_RS#45 <> H\_RS#46



4 H\_RS#46 <> H\_RS#47



4 H\_RS#47 <> H\_RS#48



4 H\_RS#48 <> H\_RS#49



4 H\_RS#49 <> H\_RS#50



4 H\_RS#50 <> H\_RS#51



4 H\_RS#51 <> H\_RS#52



4 H\_RS#52 <> H\_RS#53



4 H\_RS#53 <> H\_RS#54



4 H\_RS#54 <> H\_RS#55



4 H\_RS#55 <> H\_RS#56



4 H\_RS#56 <> H\_RS#57



4 H\_RS#57 <> H\_RS#58



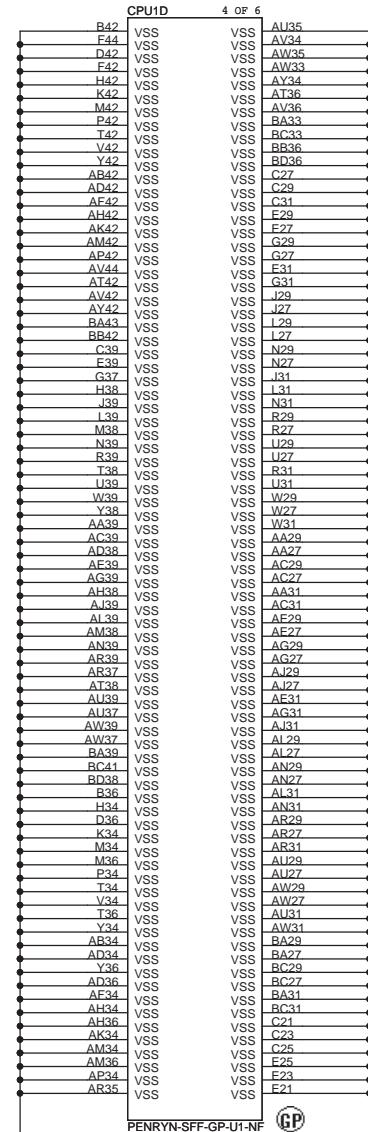
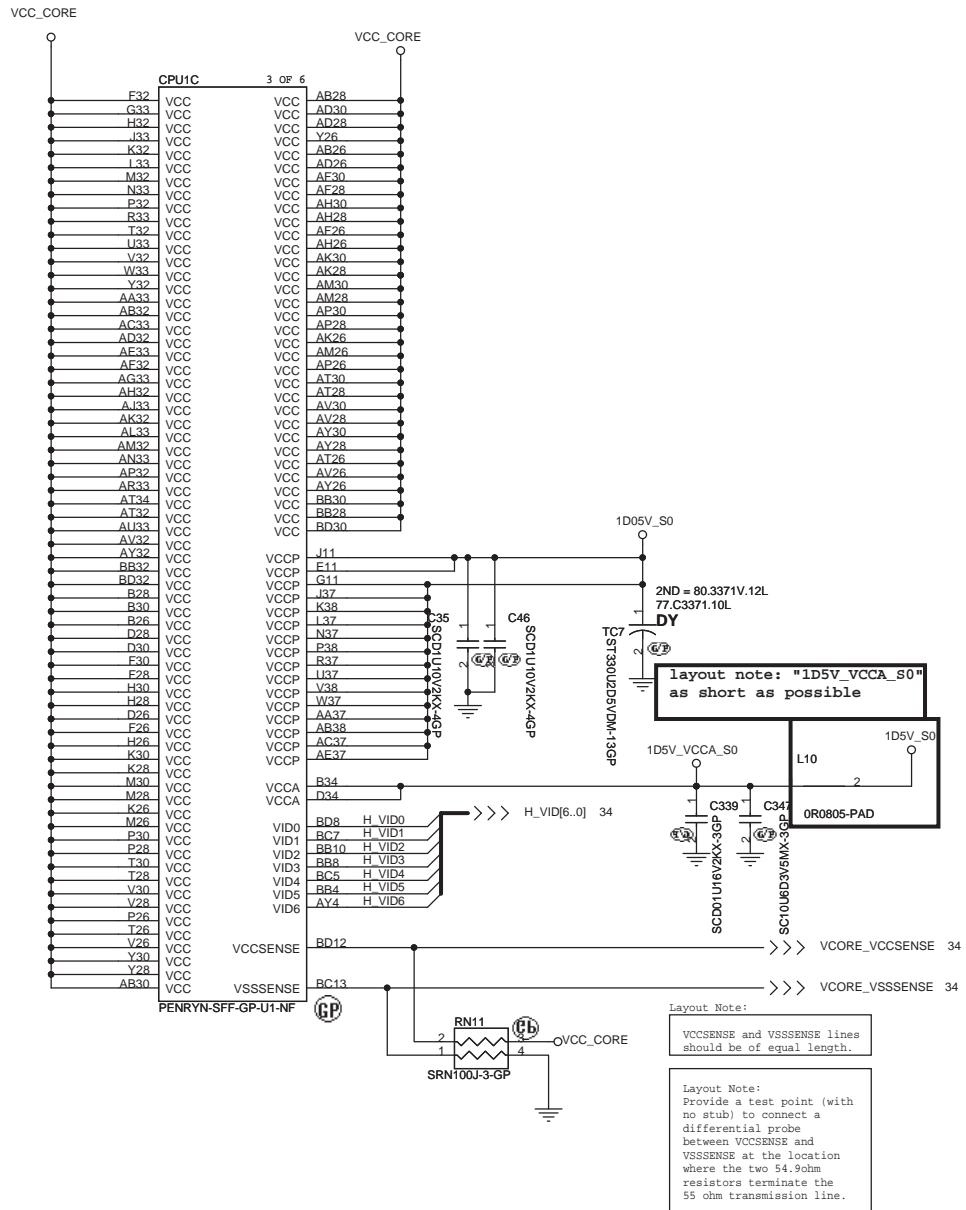
4 H\_RS#58 <> H\_RS#59

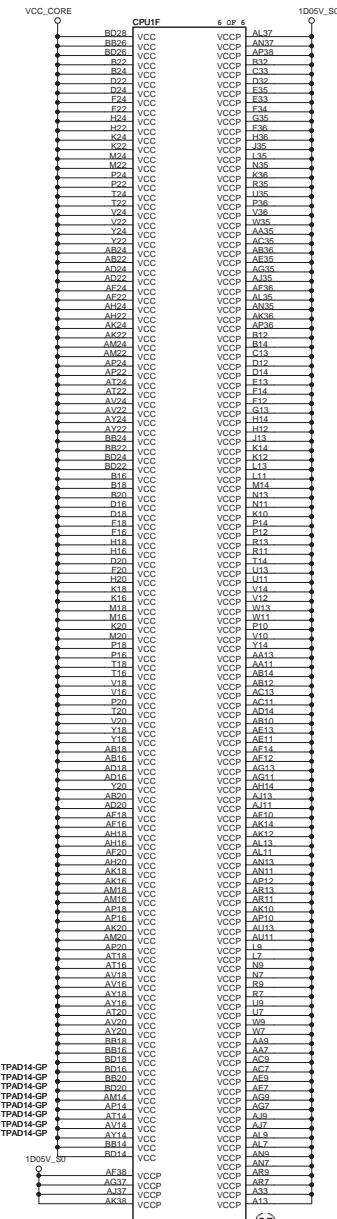
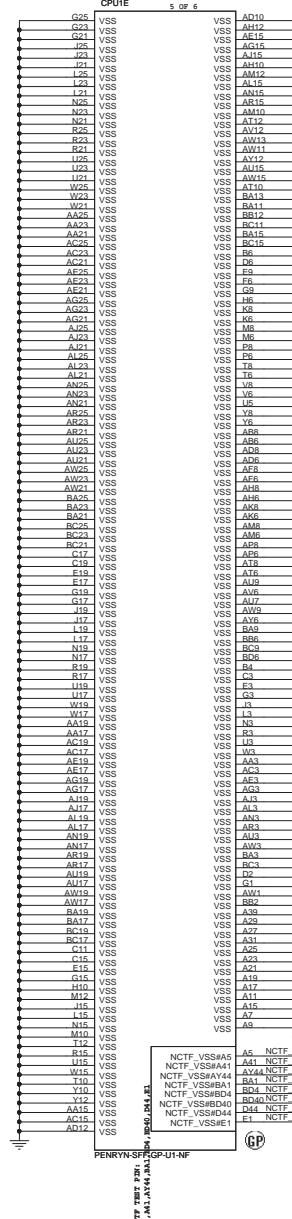
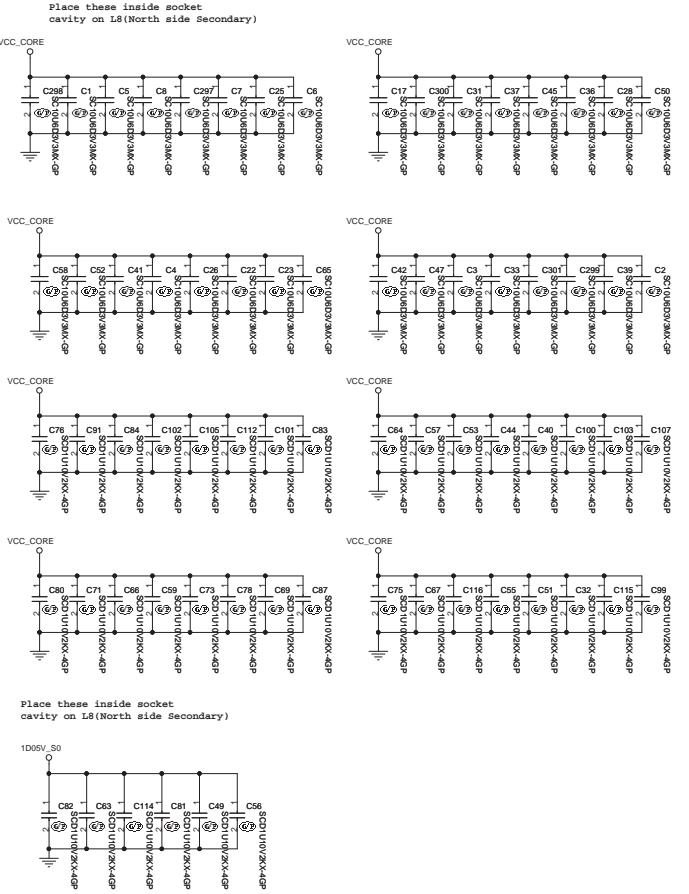


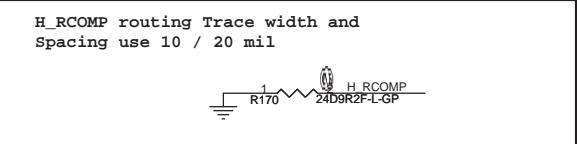
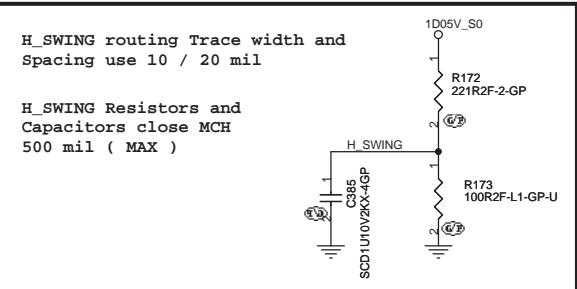
4 H\_RS#59 <> H\_RS#60



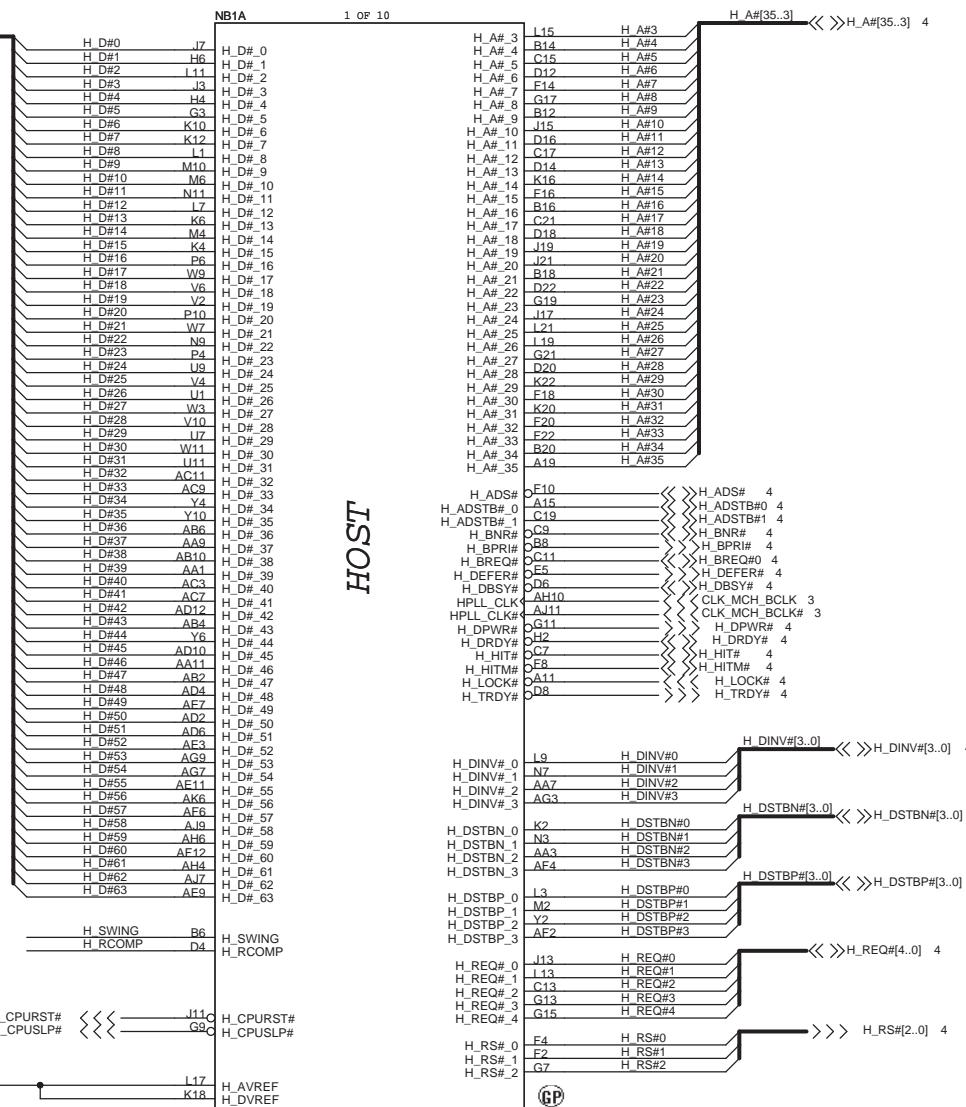
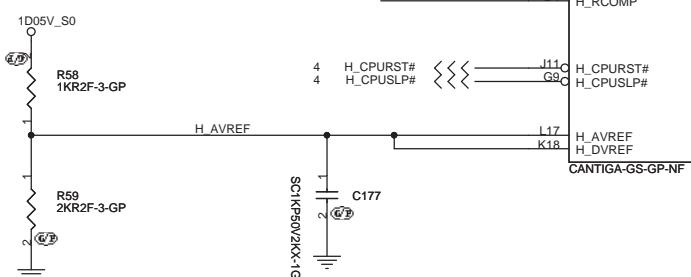
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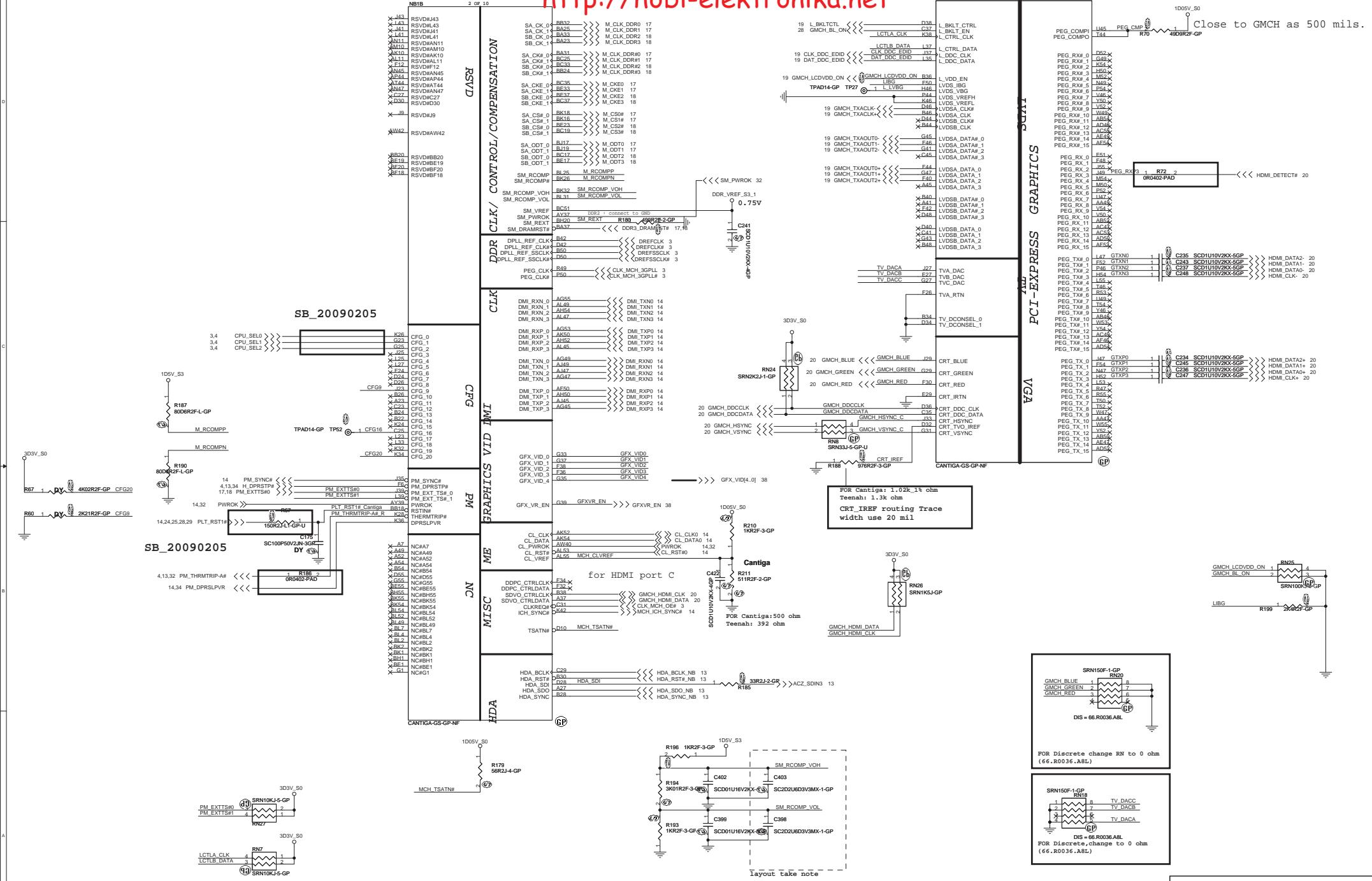


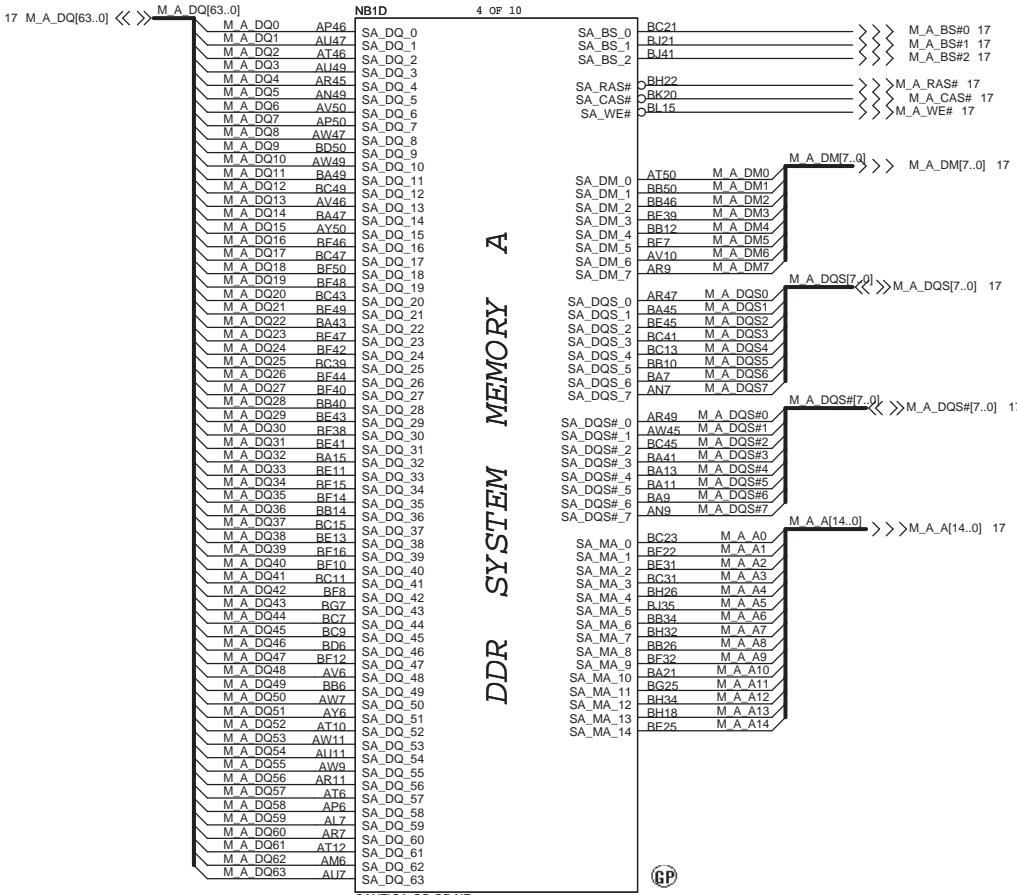
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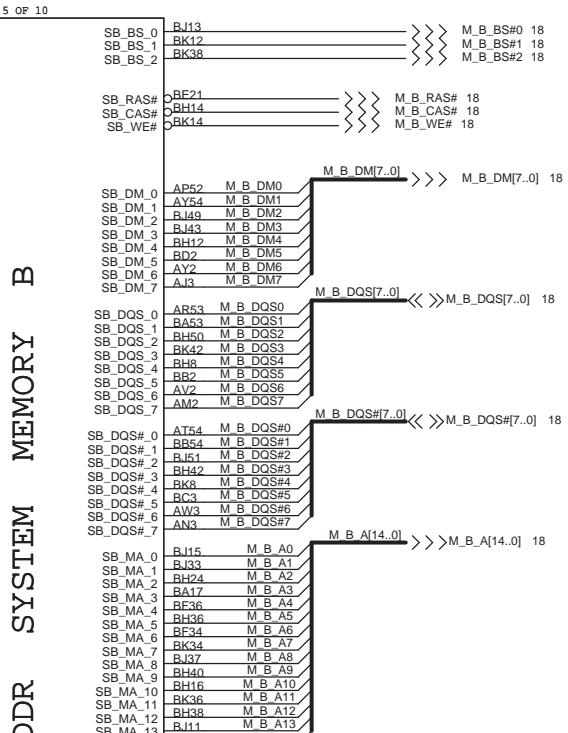
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Cantiga (1 of 6)		
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Date: Thursday, March 05, 2009	Sheet	of 40

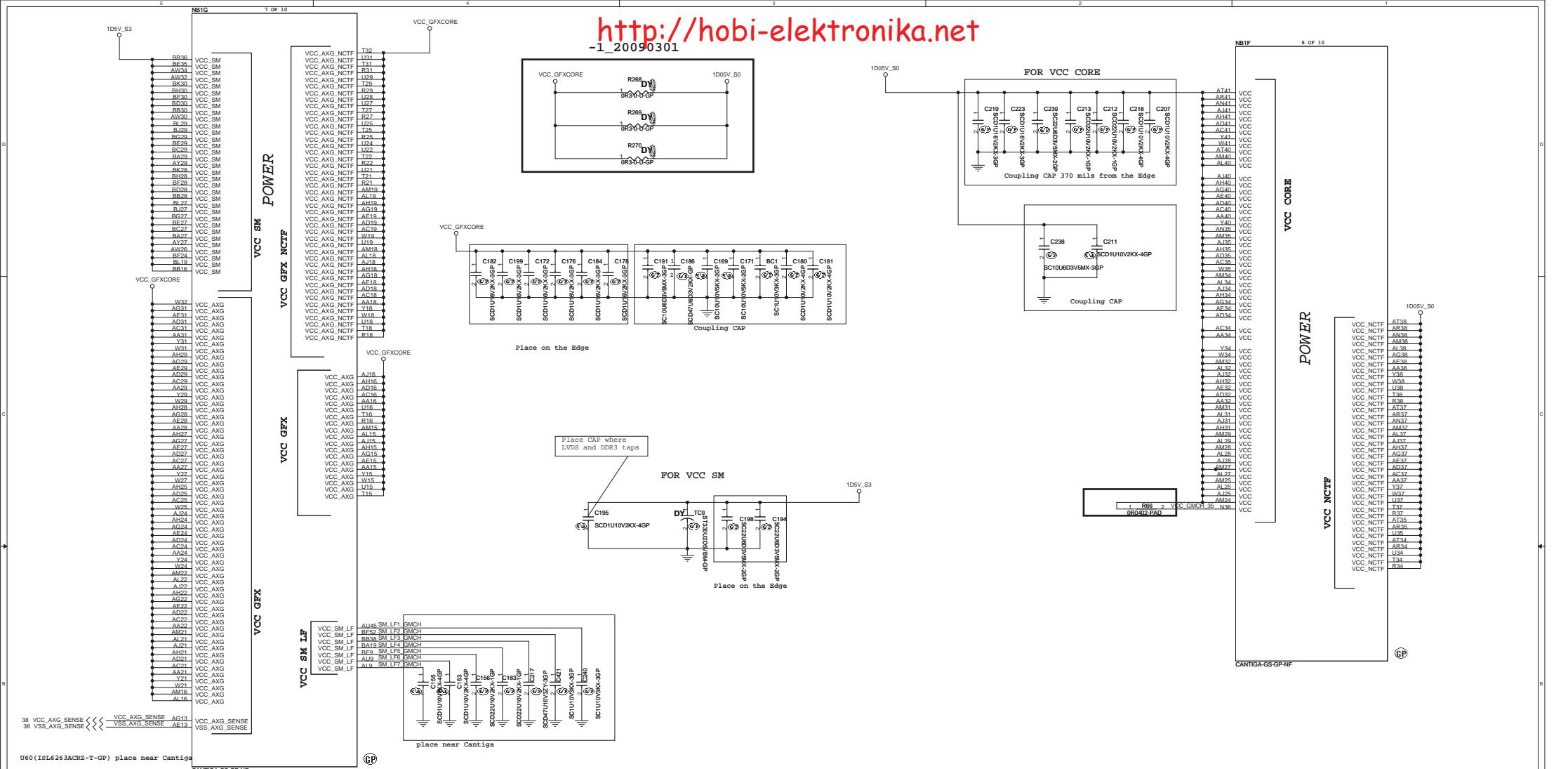


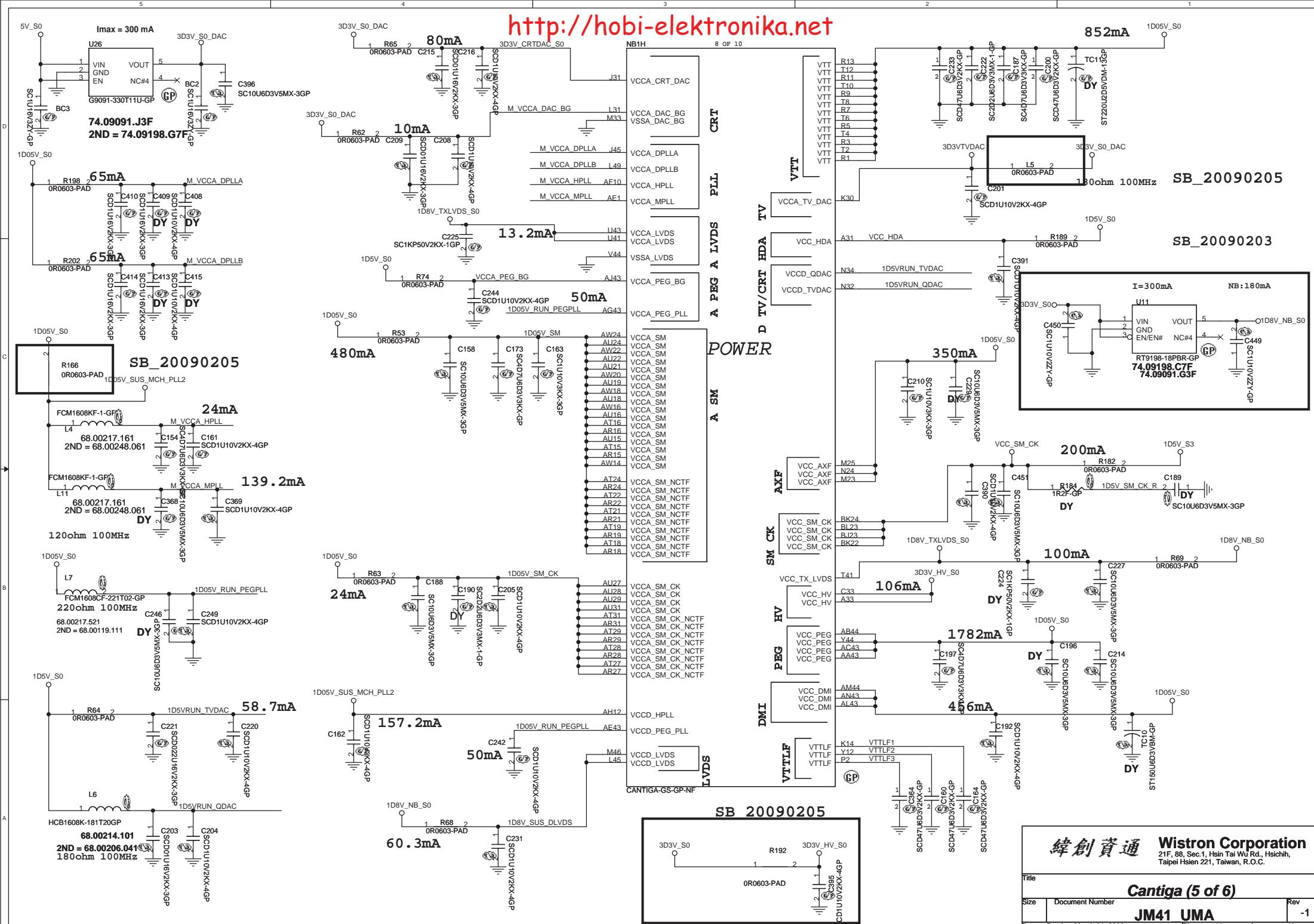


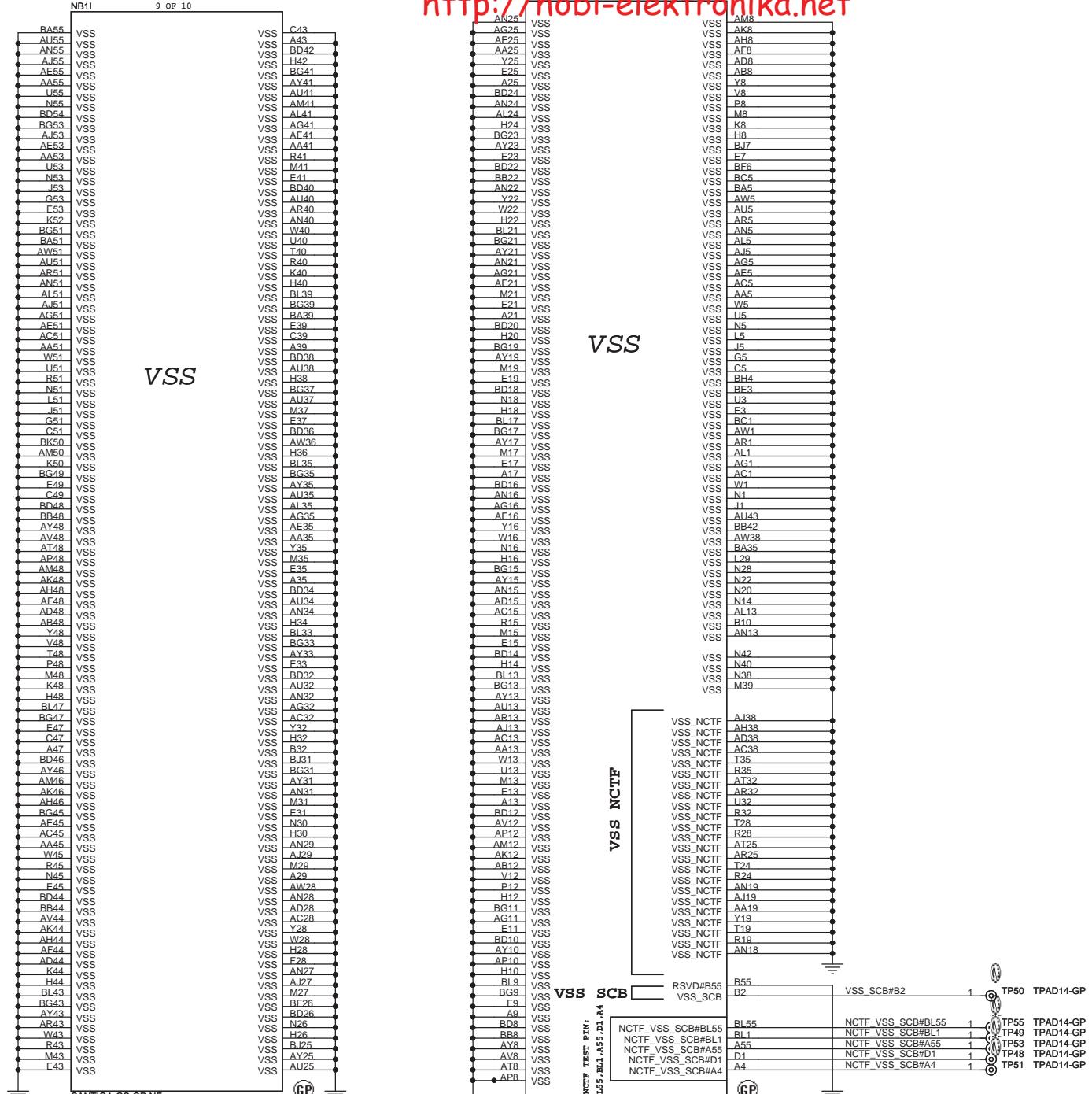
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CANTIGA-GS-GP-NF



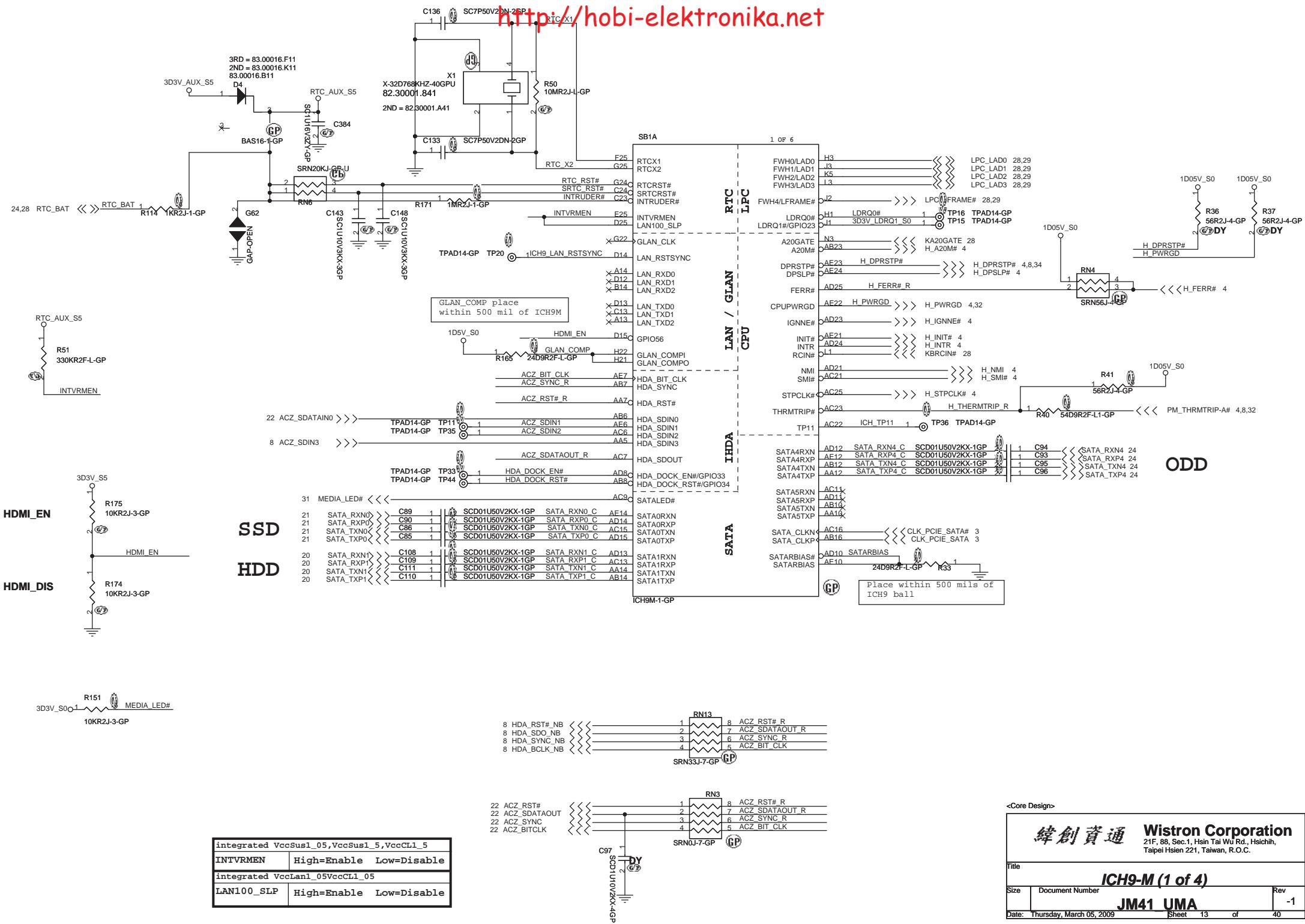


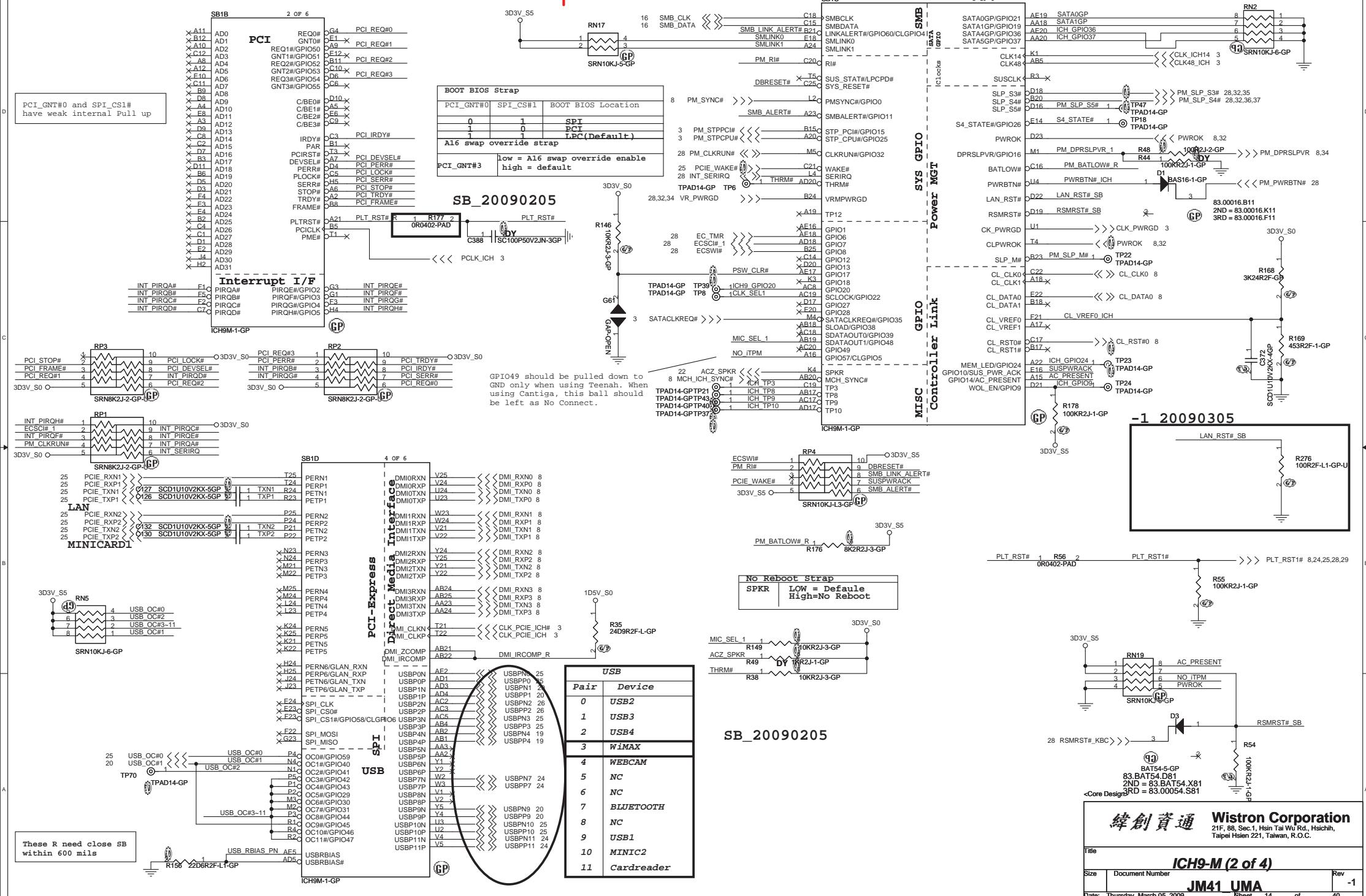




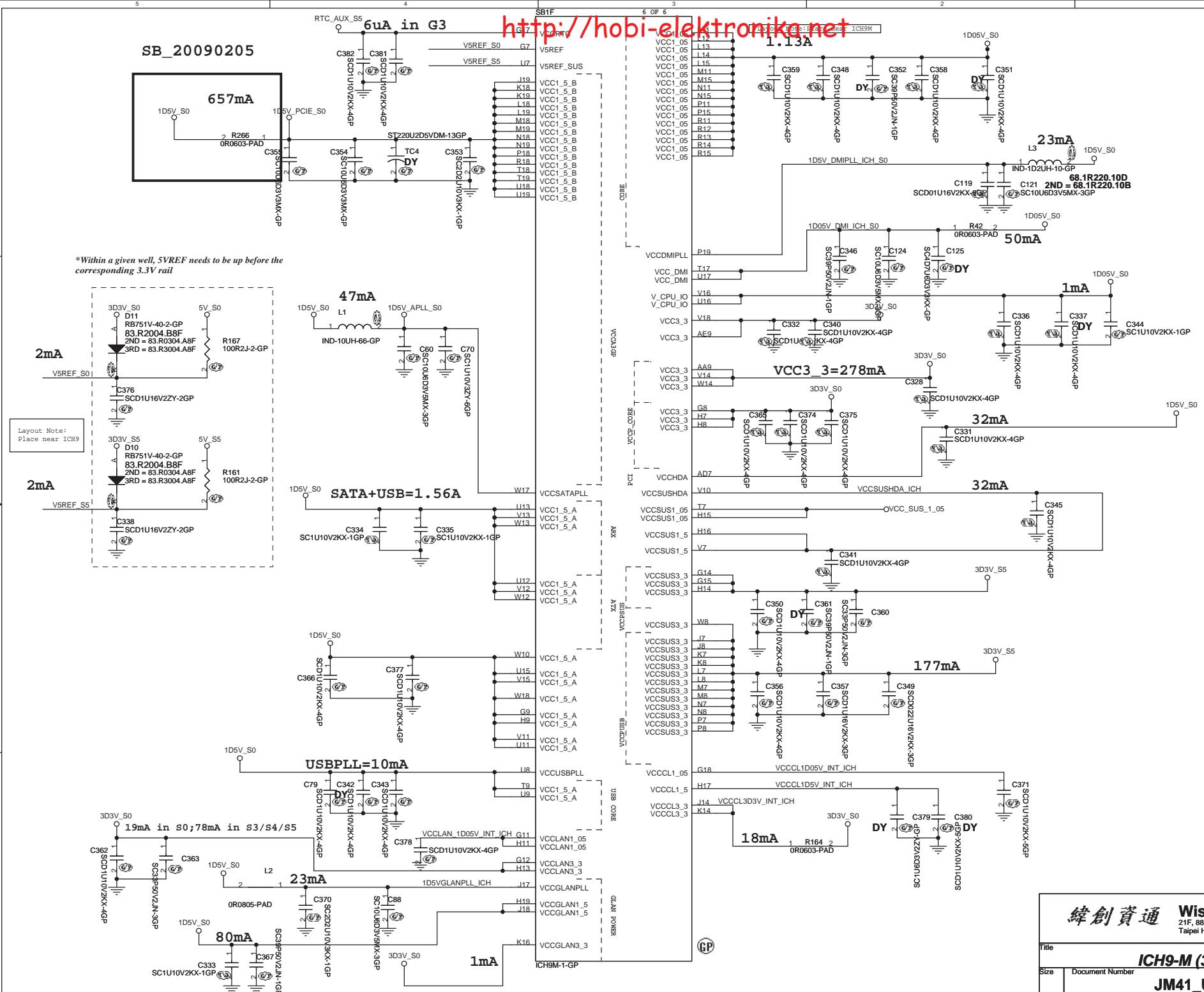
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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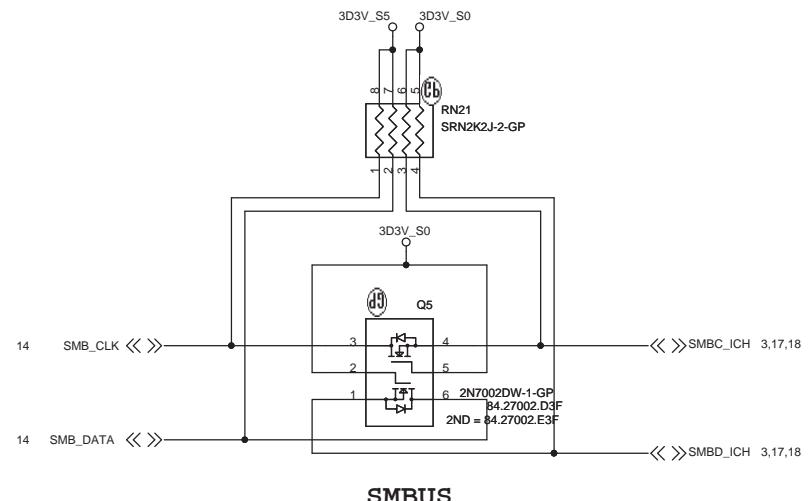
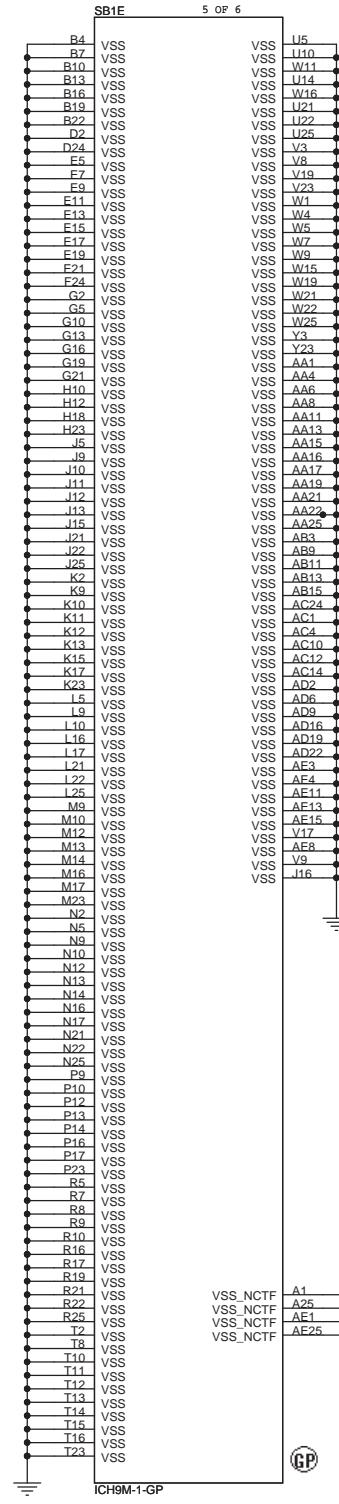
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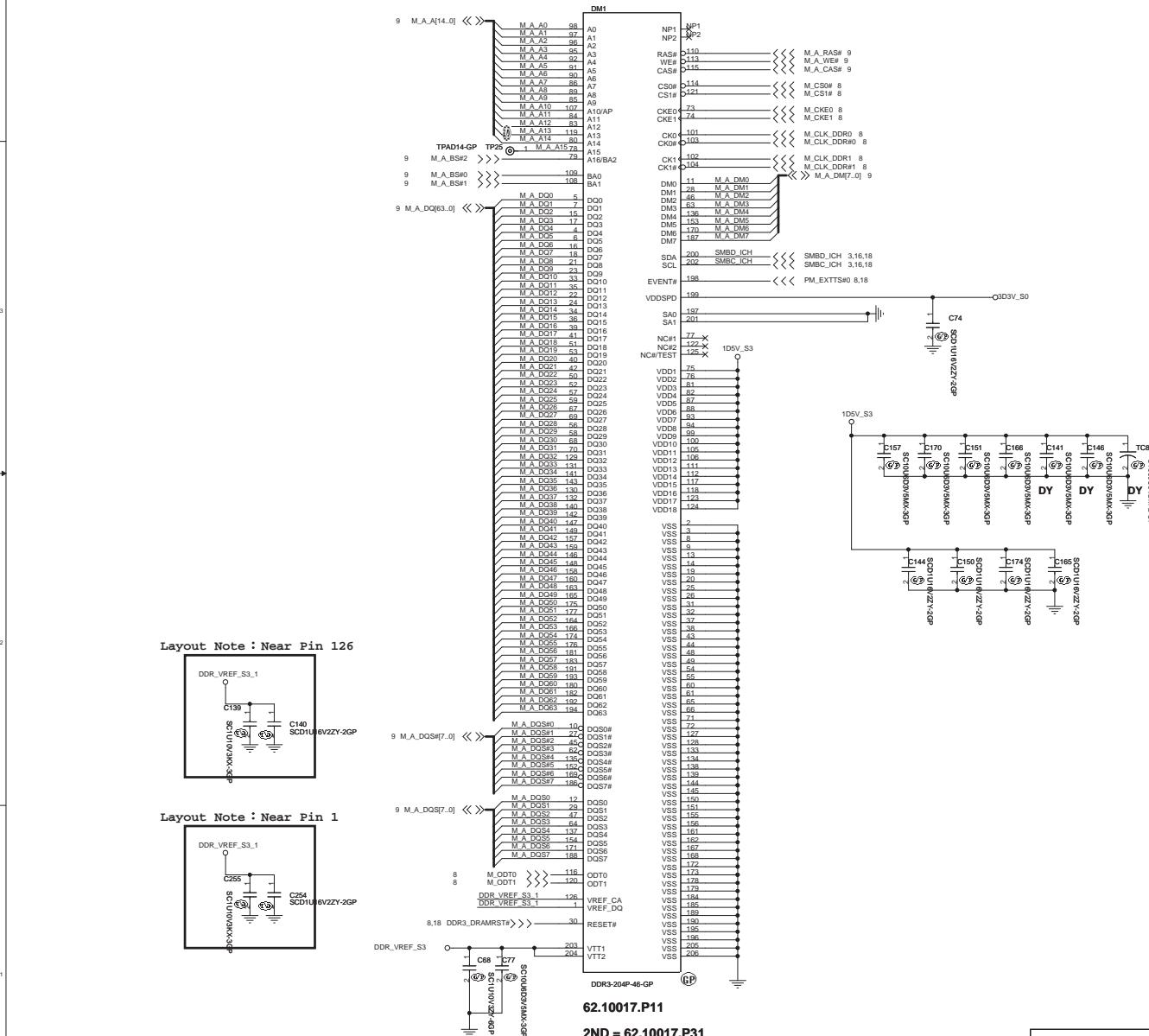


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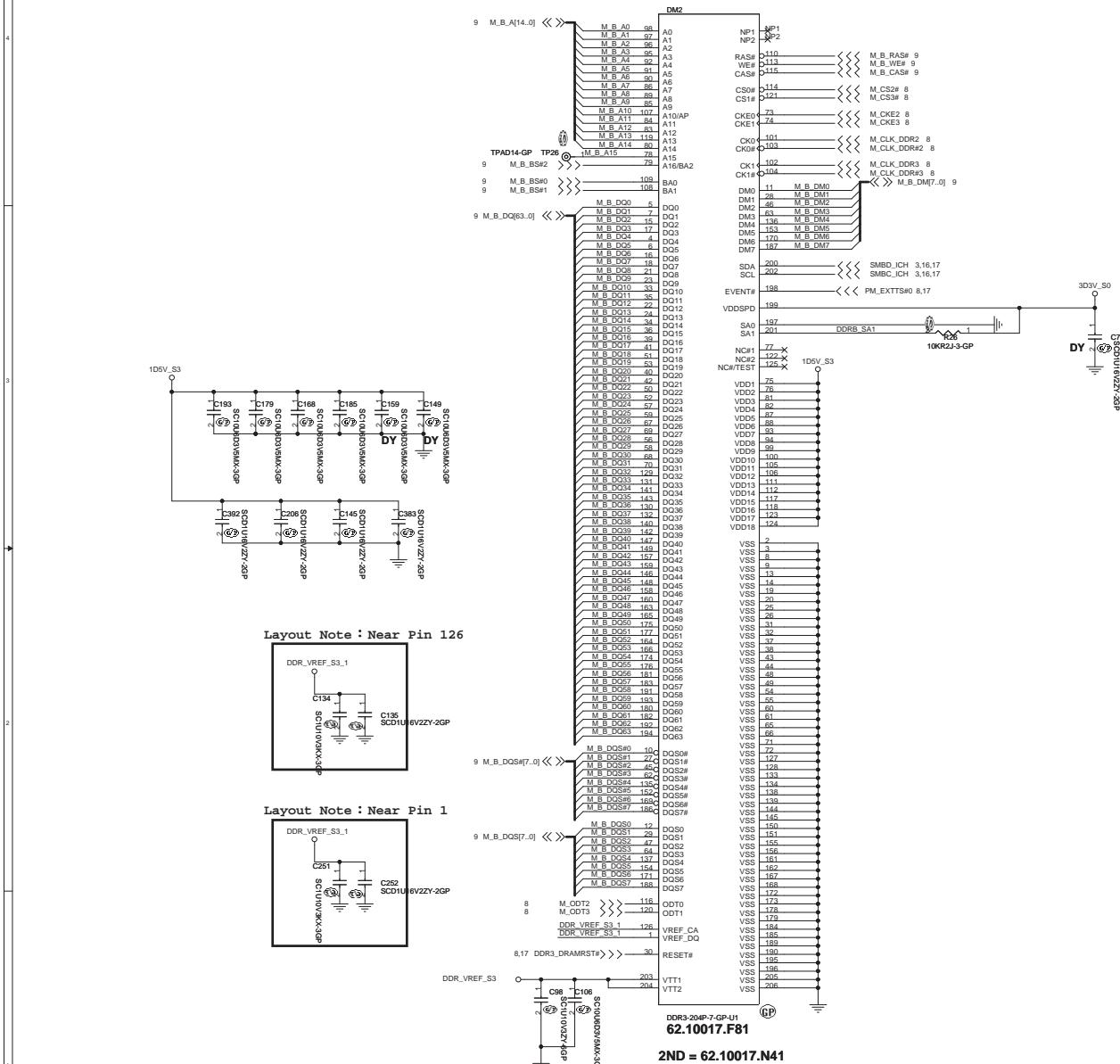


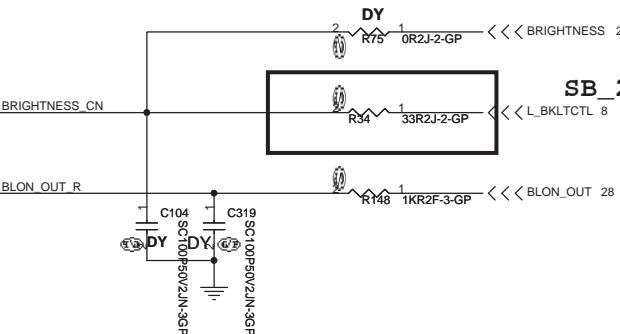
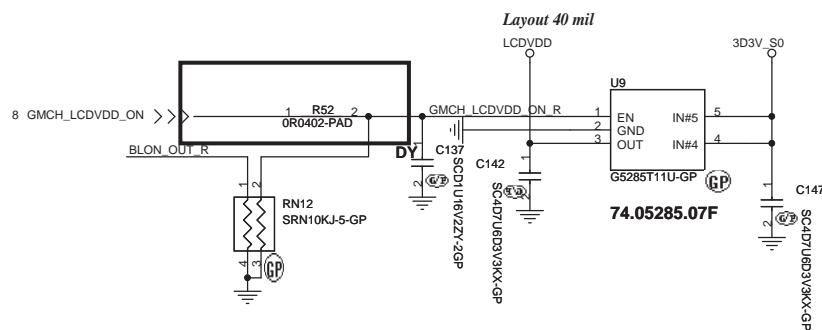
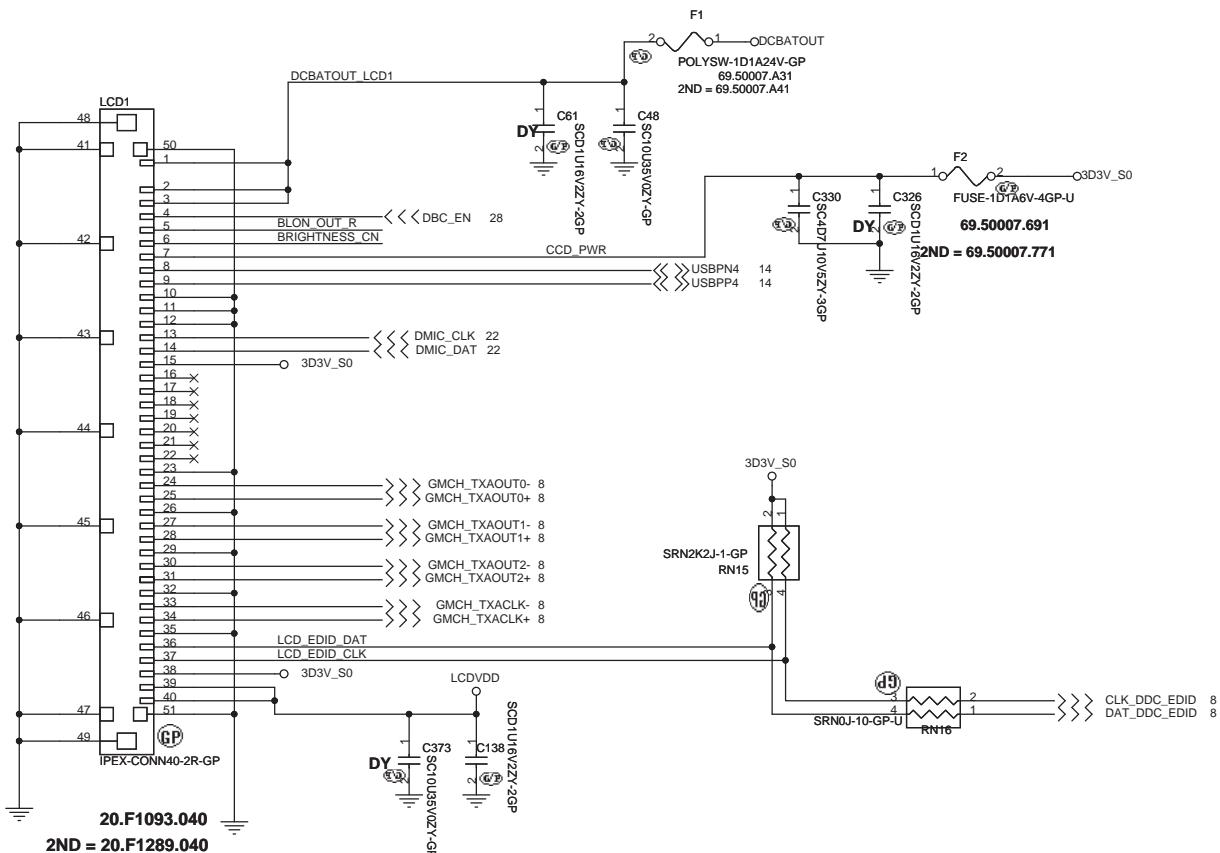


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DDR3 SOCKET\_1



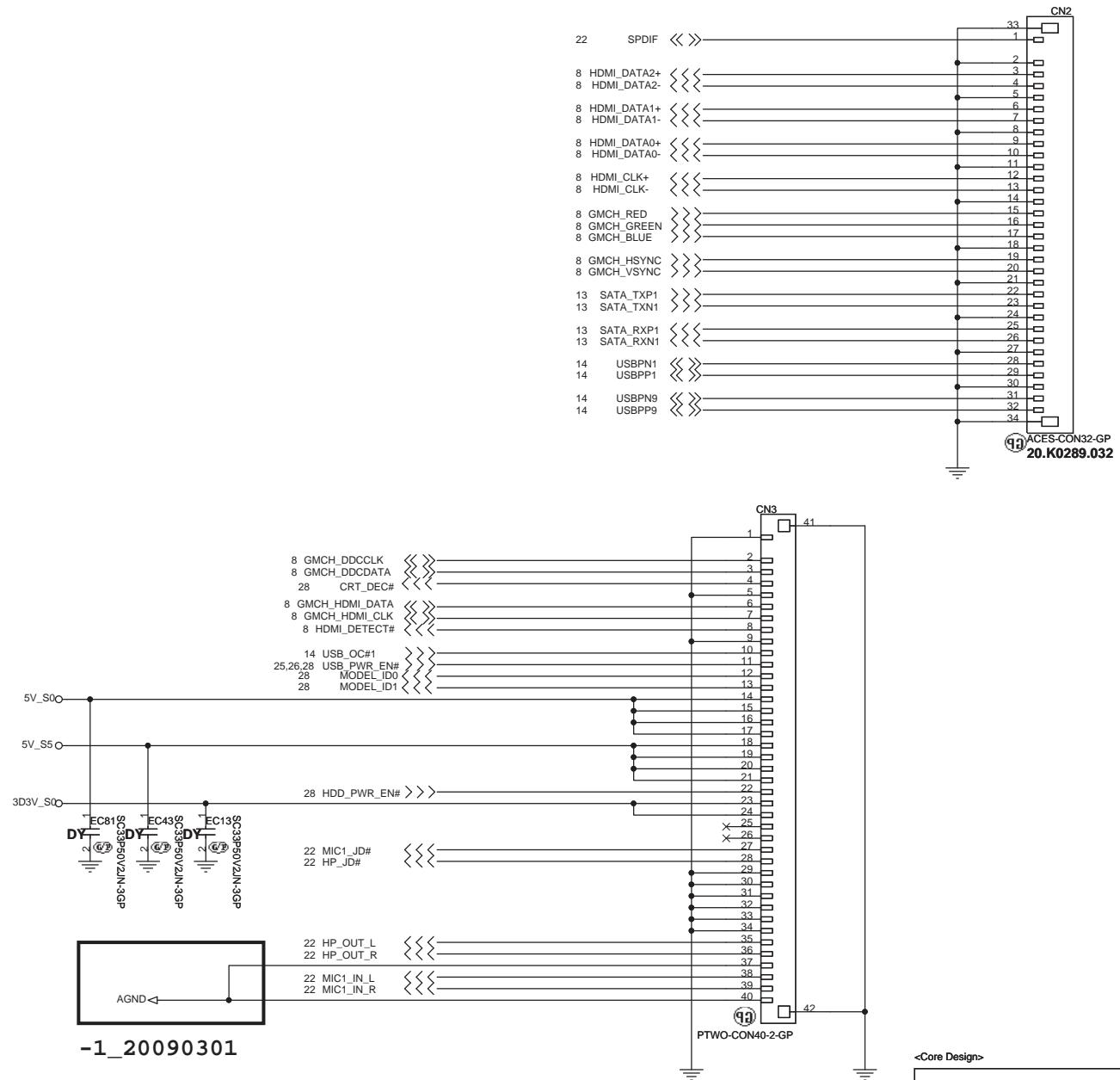
## **DDR3 SOCKET\_2**





&lt;Core Design&gt;

<b>Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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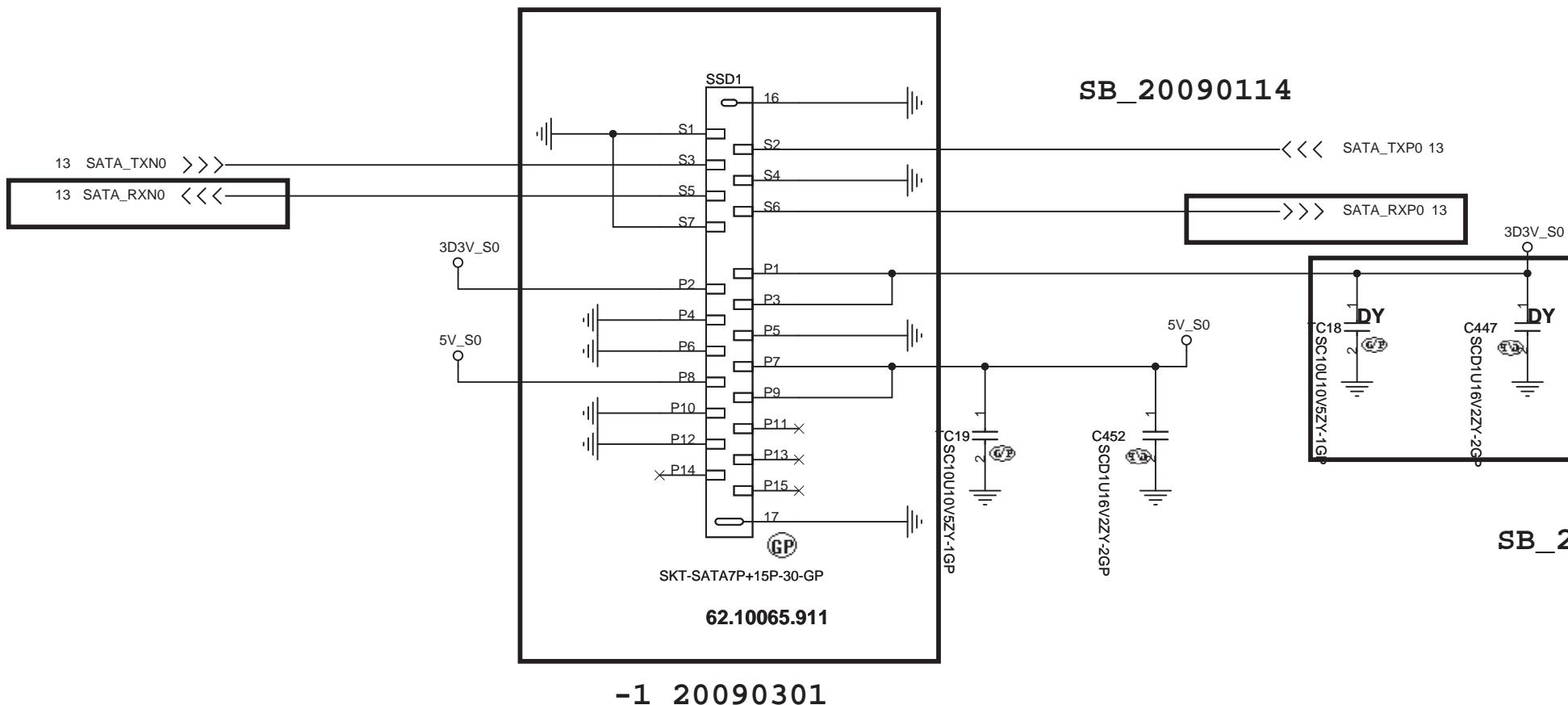


-1 20090301

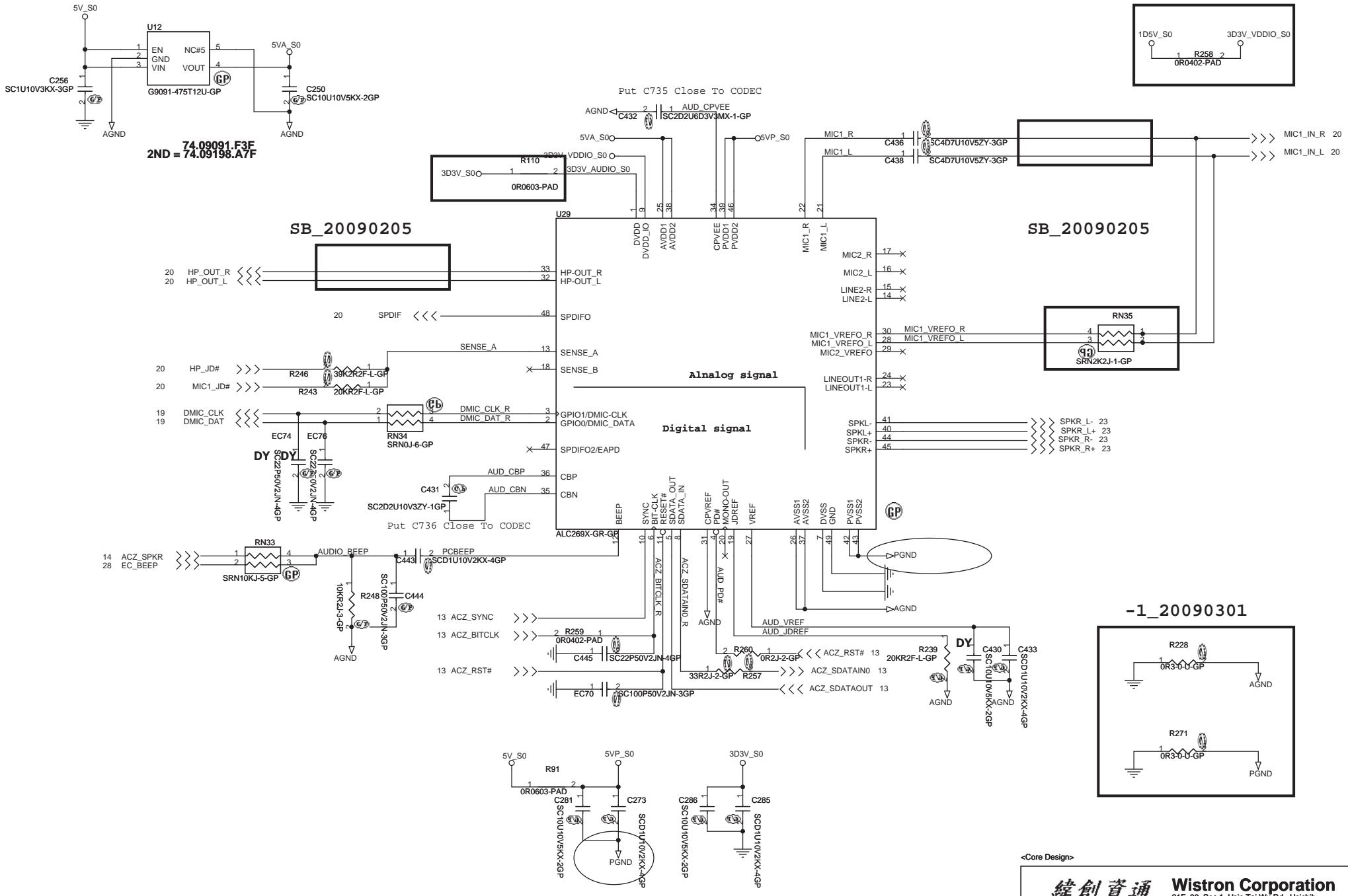
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**2ND = 20.K0420.040**

<Core Design>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title				
<b>CRT BD CONN</b>				
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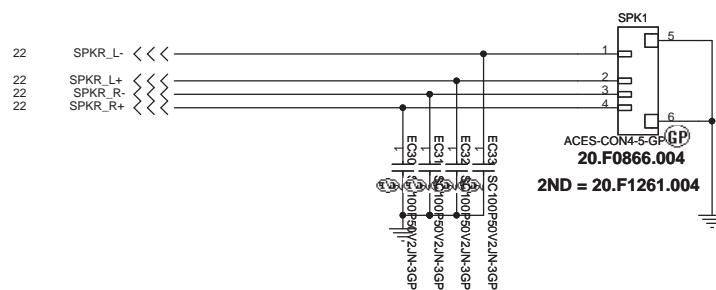
# SSD SATA Connector



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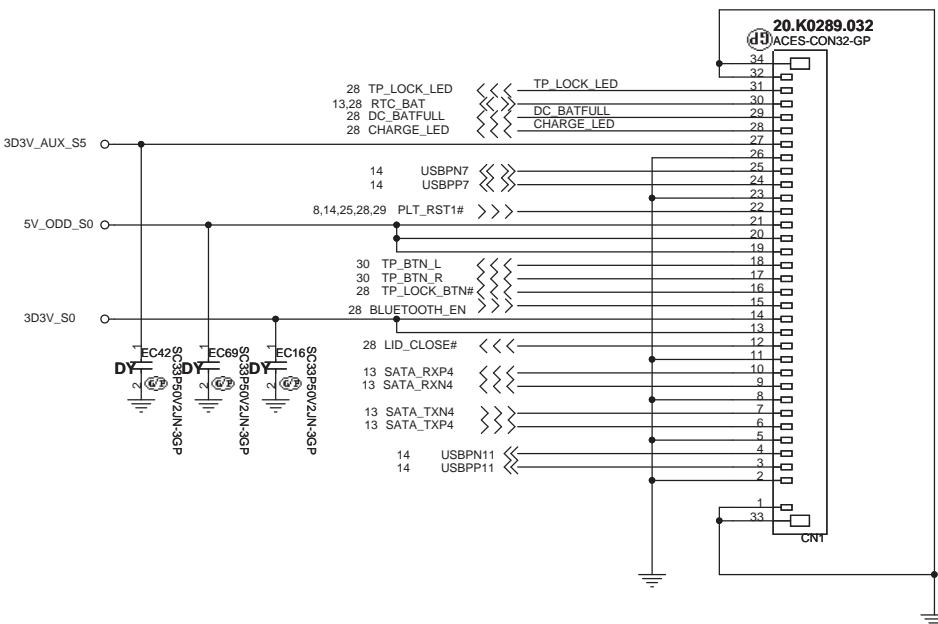


## Internal Speaker



<Core Design>

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Title	
AUDIO JACK	
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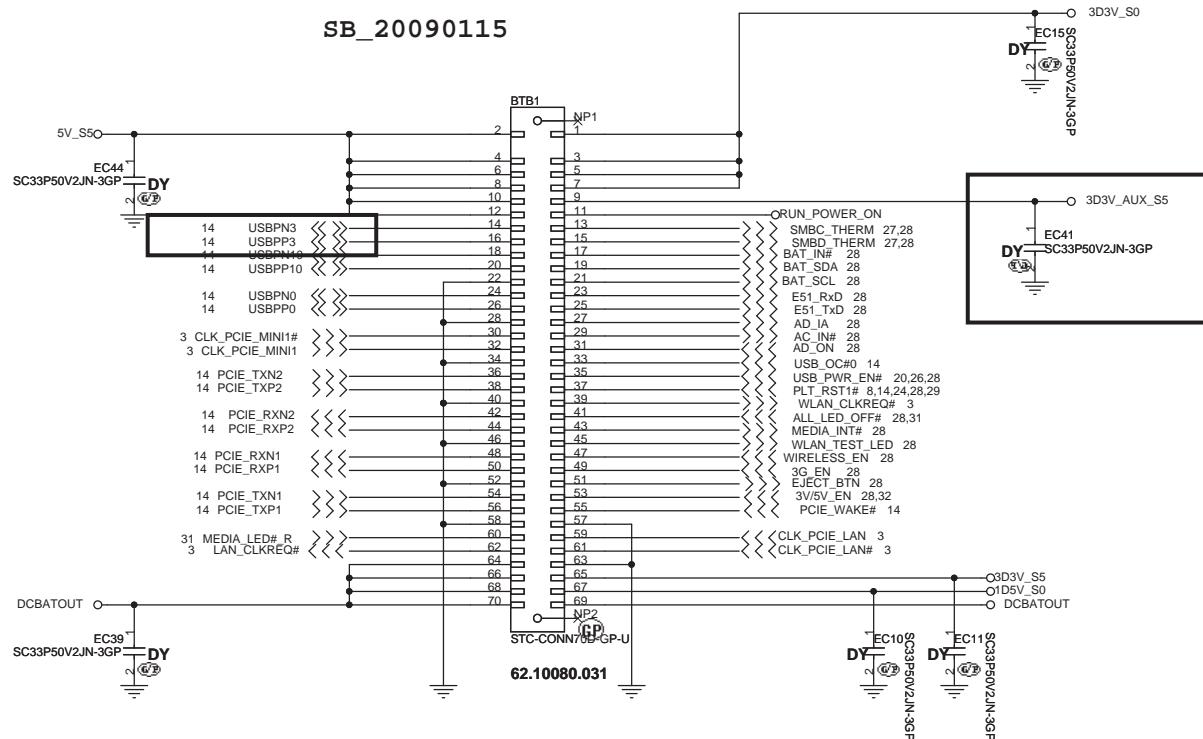
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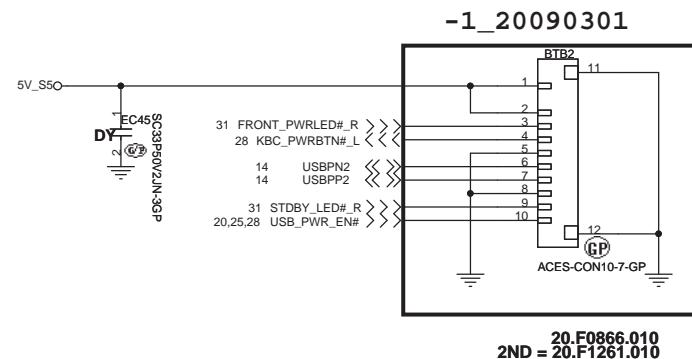
**緯創資通** Wistron Corporation  
21F, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

**Title**

## **CARDREADER BD CONN**

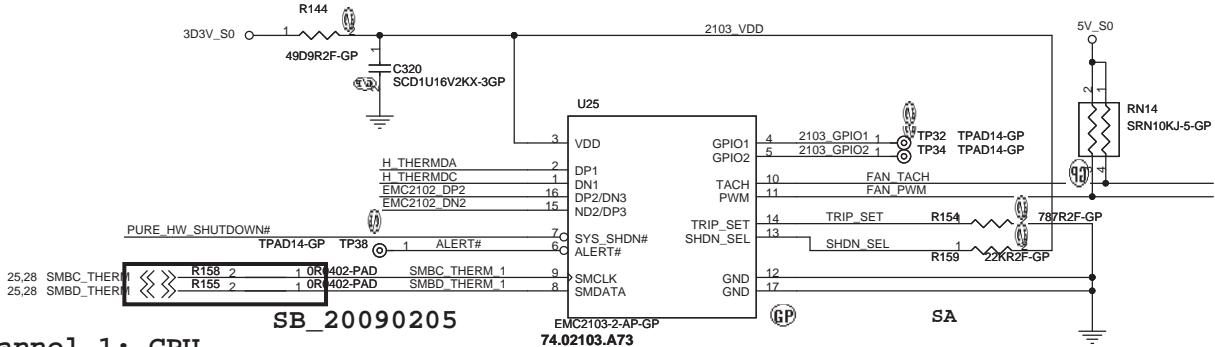
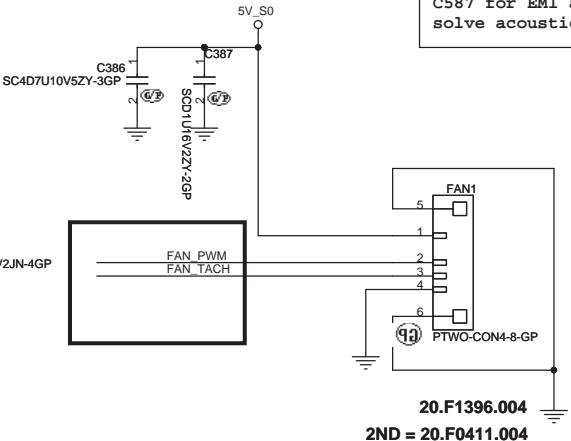
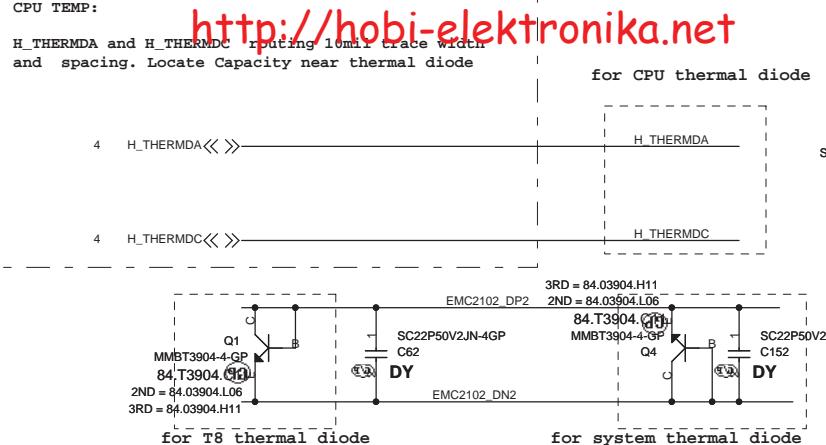
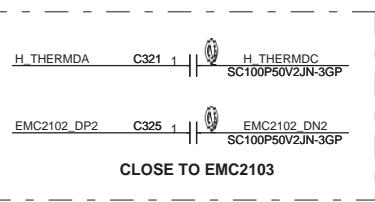
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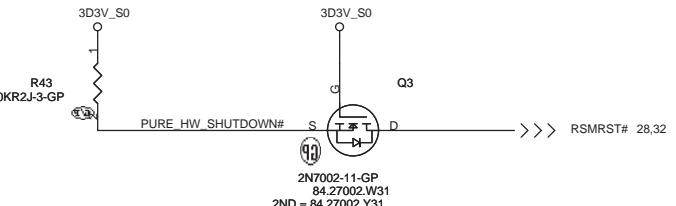
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Channel 1: CPU  
Channel 2: Palmrest  
Channel 3: T8

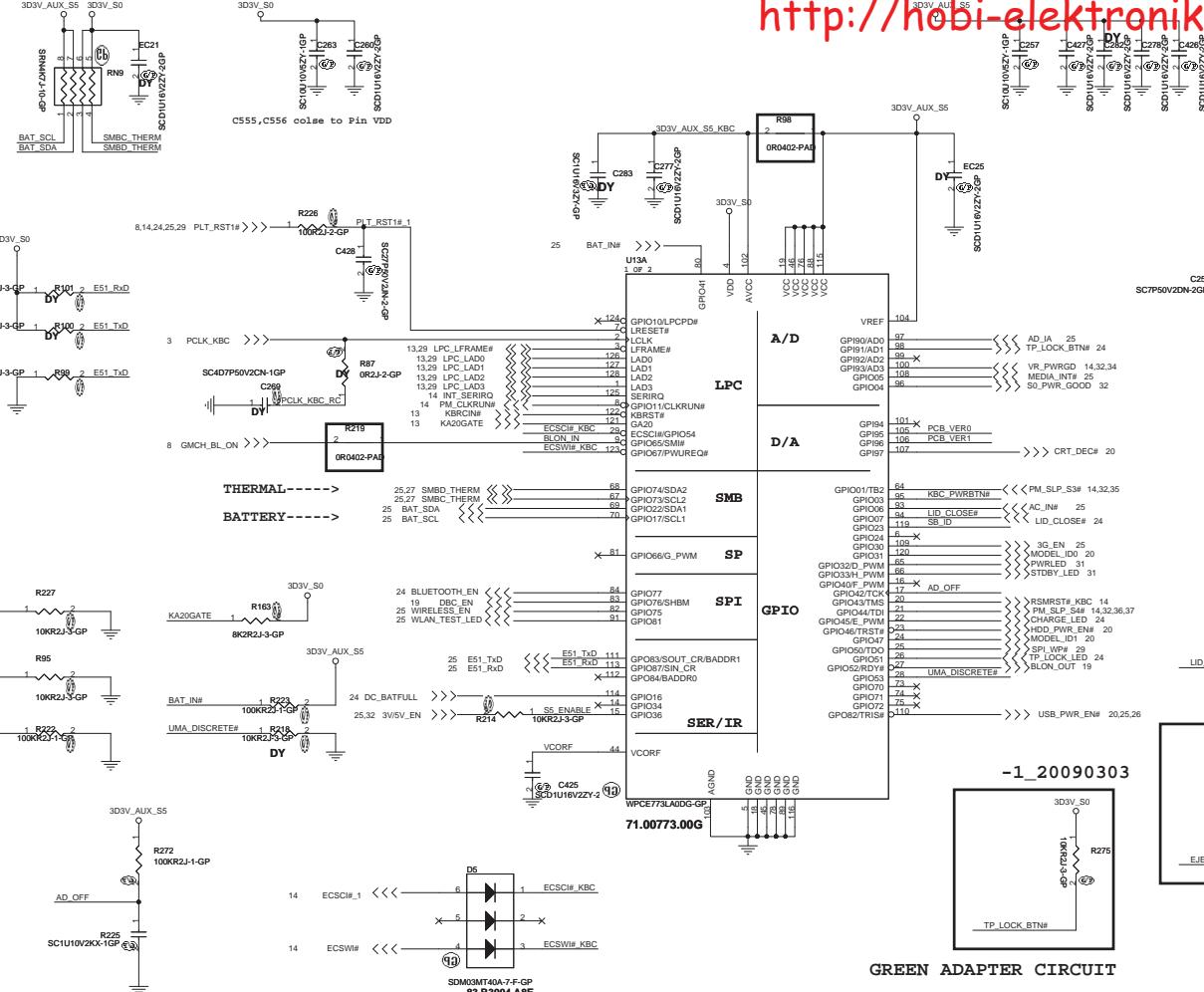
ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL



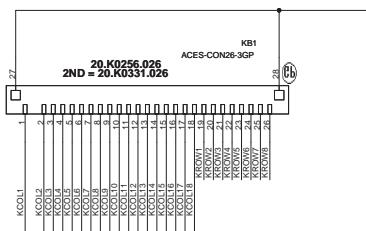
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

<Core Design>



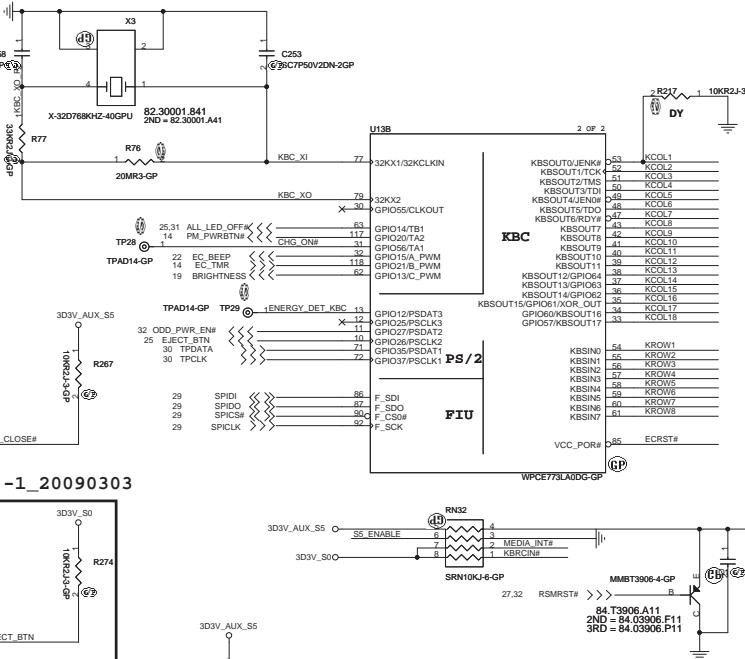
### Internal Keyboard Connector



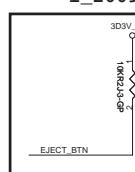
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24



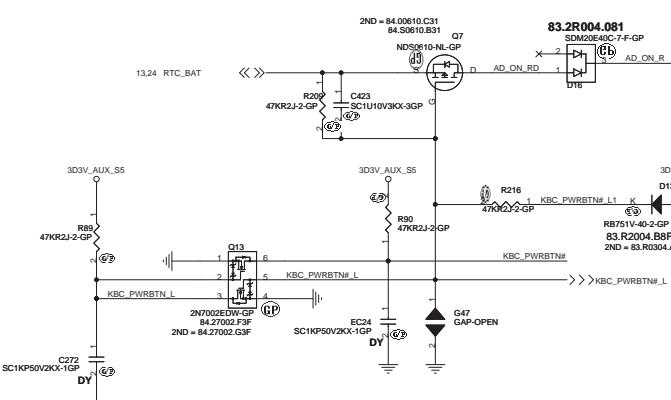
24 1



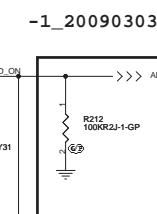
-1\_20090303



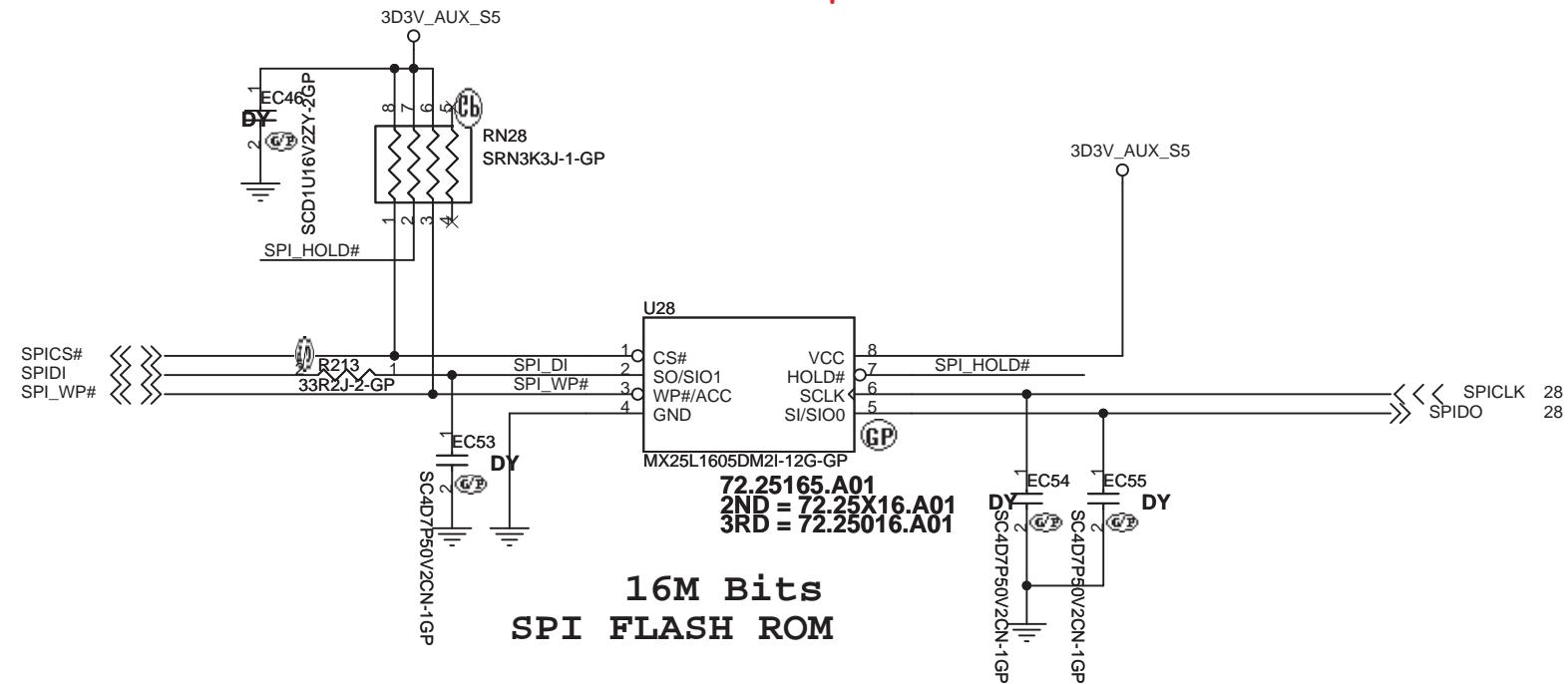
### GREEN ADAPTER CIRCUIT



-1\_20090303

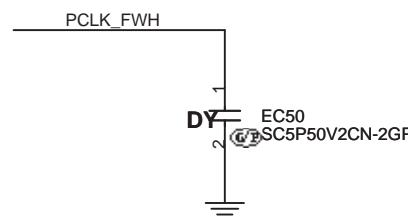


-1\_20090303



### GOLDEN FINGER FOR DEBUG BOARD

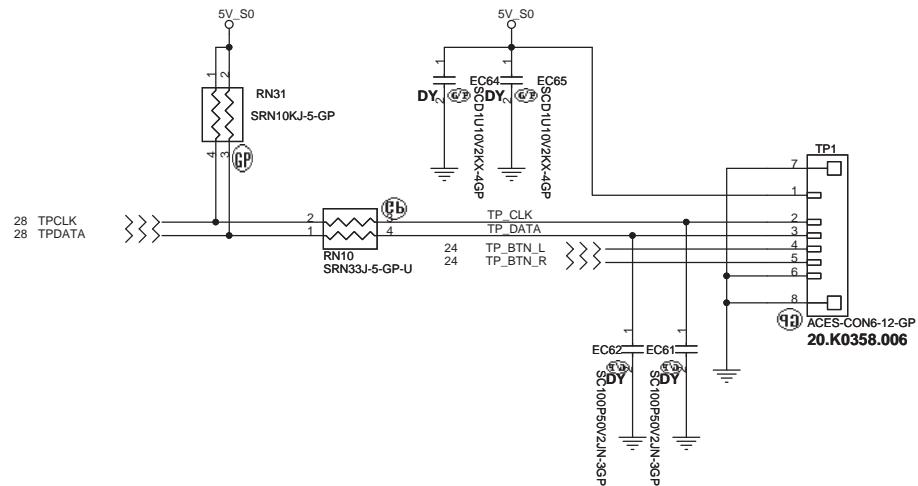
13,28	LPC_LAD0	LPC_LAD0	1	TP58	TPAD30-1-GP
13,28	LPC_LAD1	LPC_LAD1	1	TP59	TPAD30-1-GP
13,28	LPC_LAD2	LPC_LAD2	1	TP61	TPAD30-1-GP
13,28	LPC_LAD3	LPC_LAD3	1	TP60	TPAD30-1-GP
13,28	LPC_LFRAME#	LPC_LFRAME#	1	TP56	TPAD30-1-GP
8,14,24,25,28	PLT_RST1#	PLT_RST1#	1	TP54	TPAD30-1-GP
3	PCLK_FWH	PCLK_FWH	1	TP57	TPAD30-1-GP

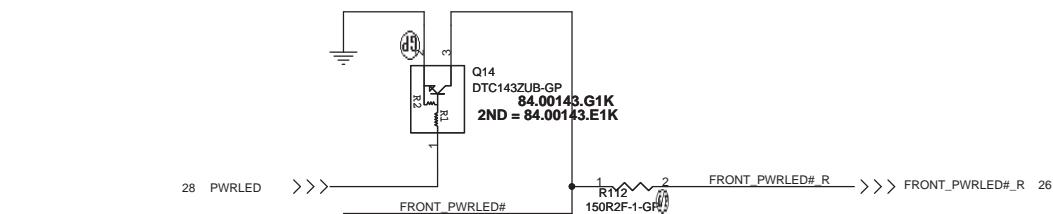


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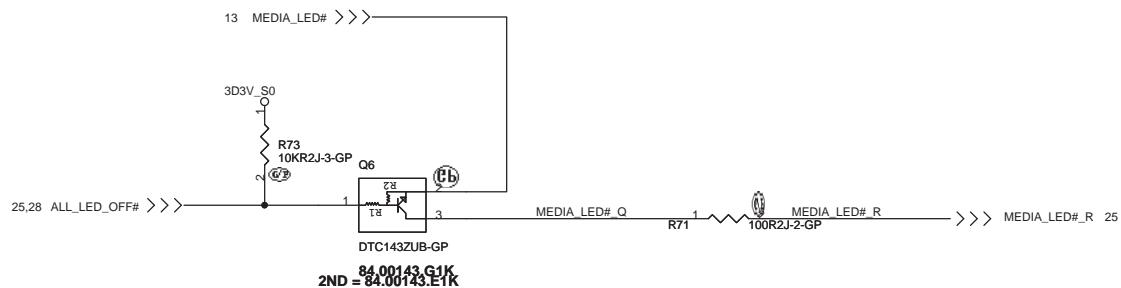
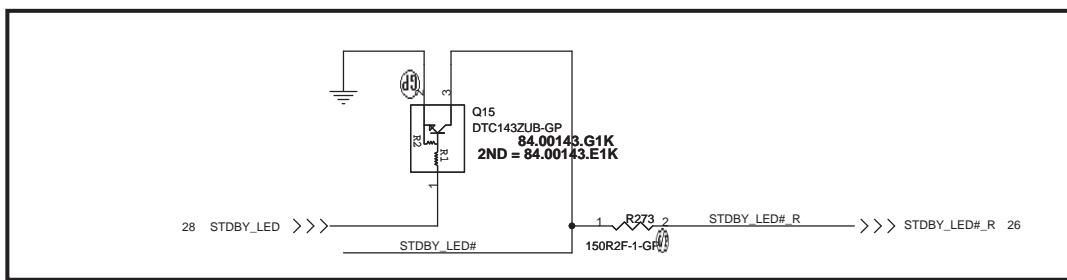
<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b> BIOS</b>	
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## TOUCH PAD



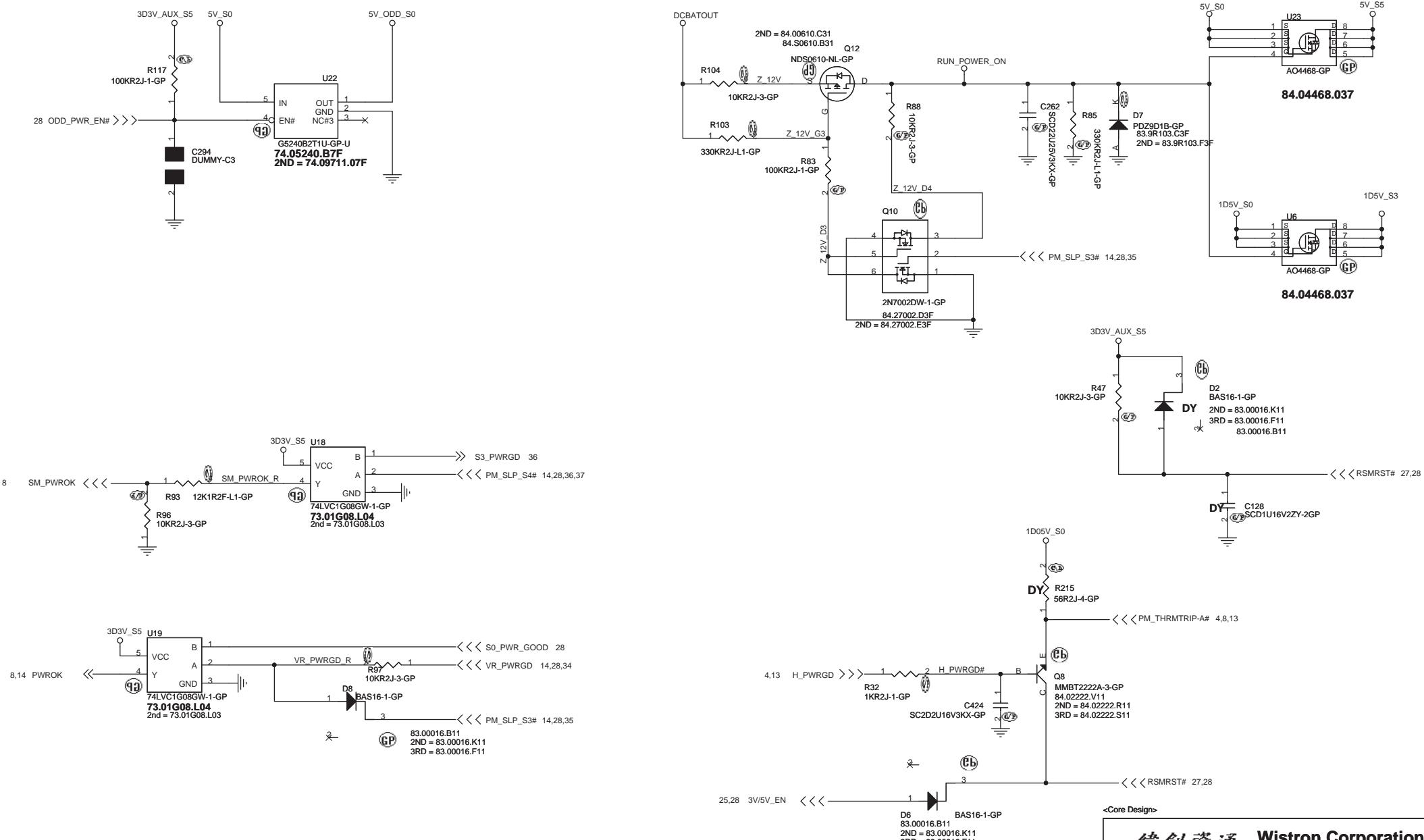


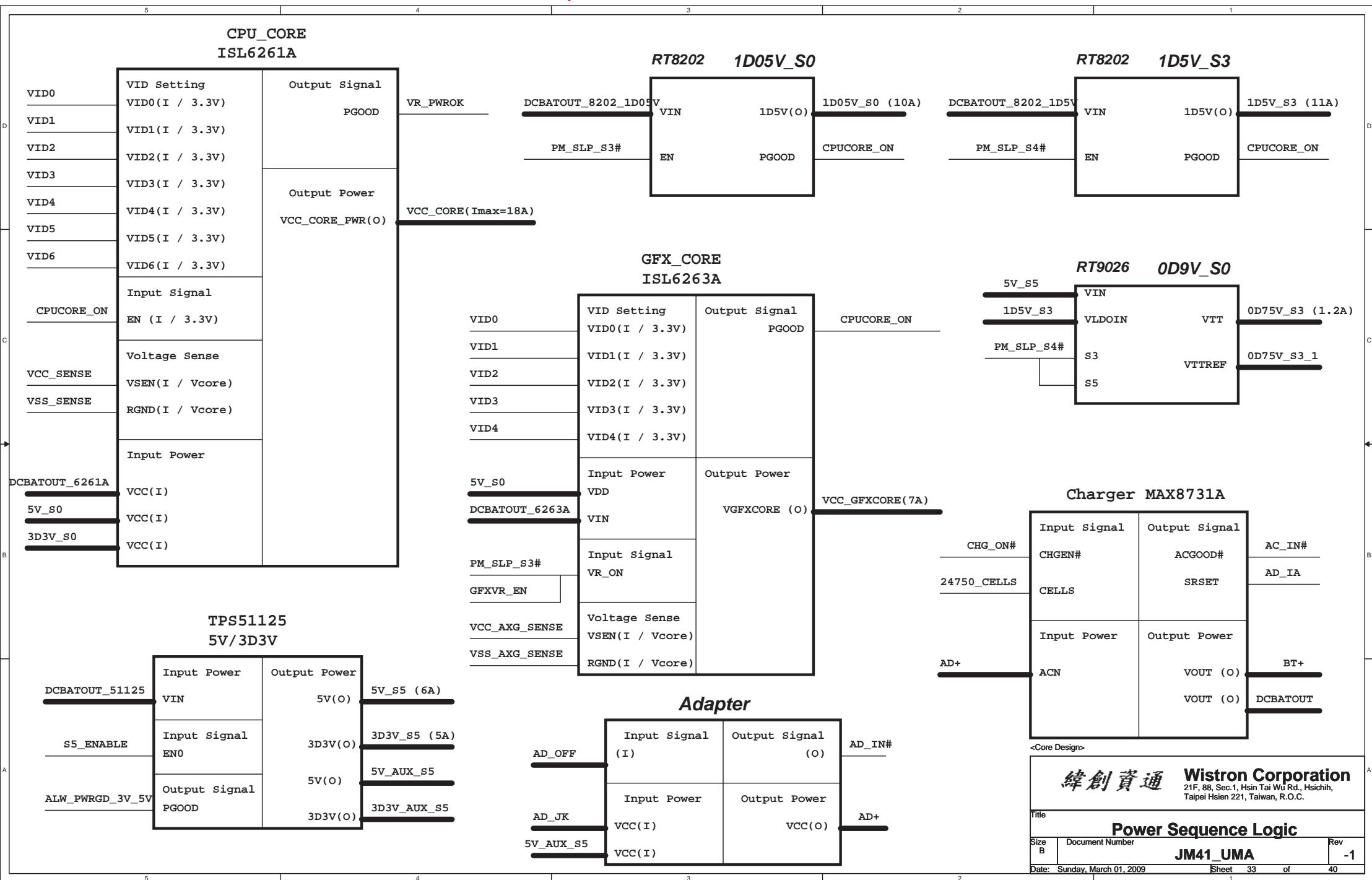
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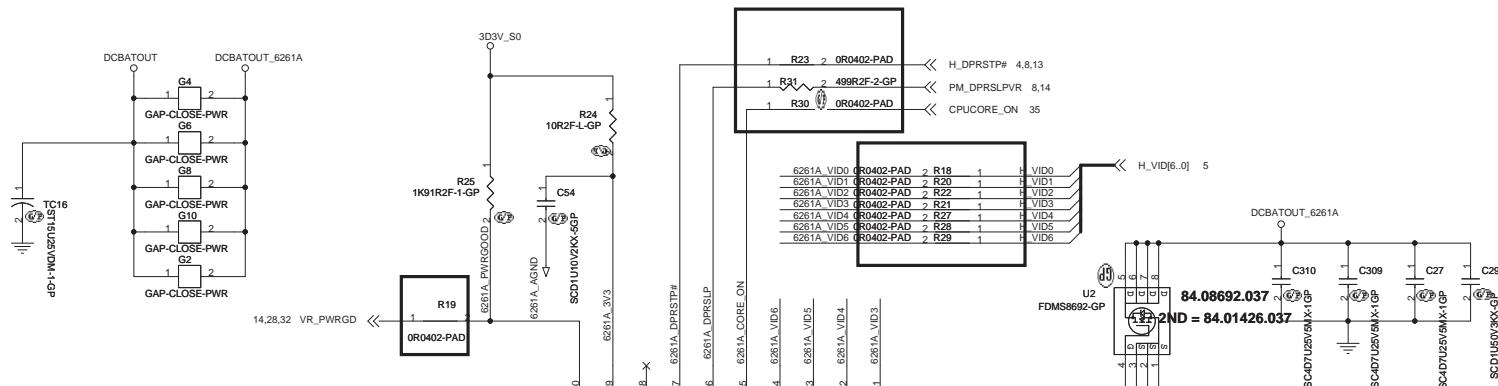
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<b>緯創資通 Wistron Corporation</b> <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>		
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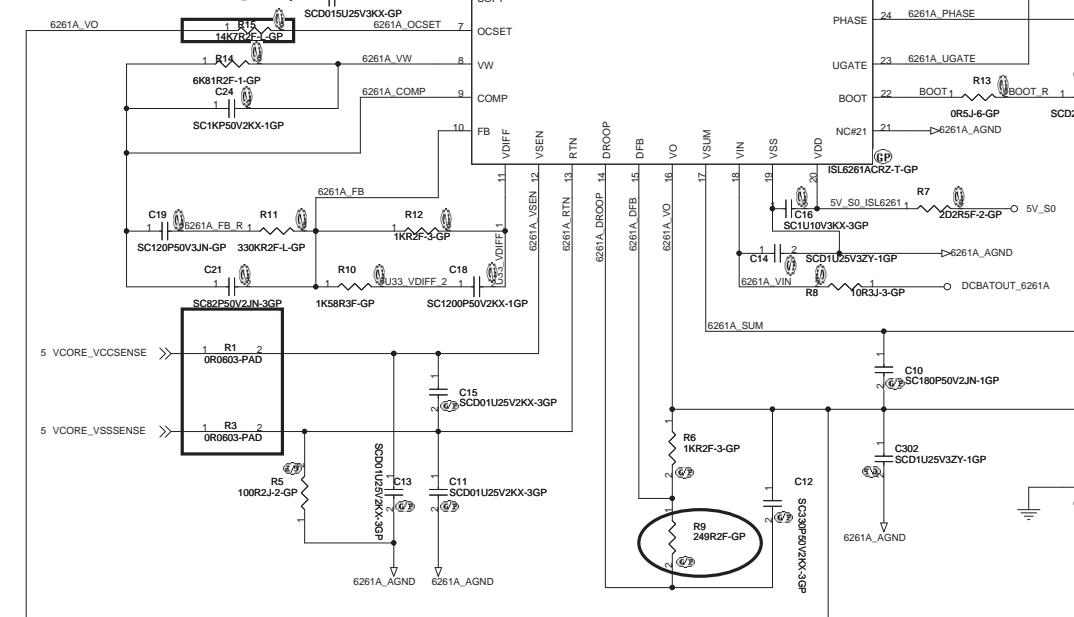




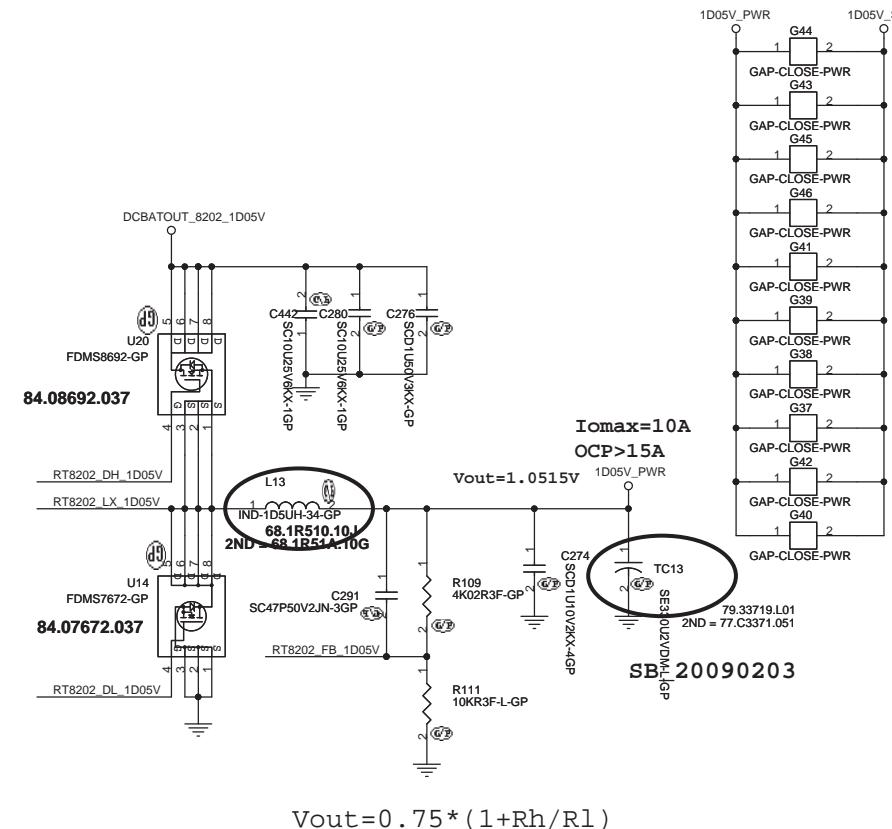
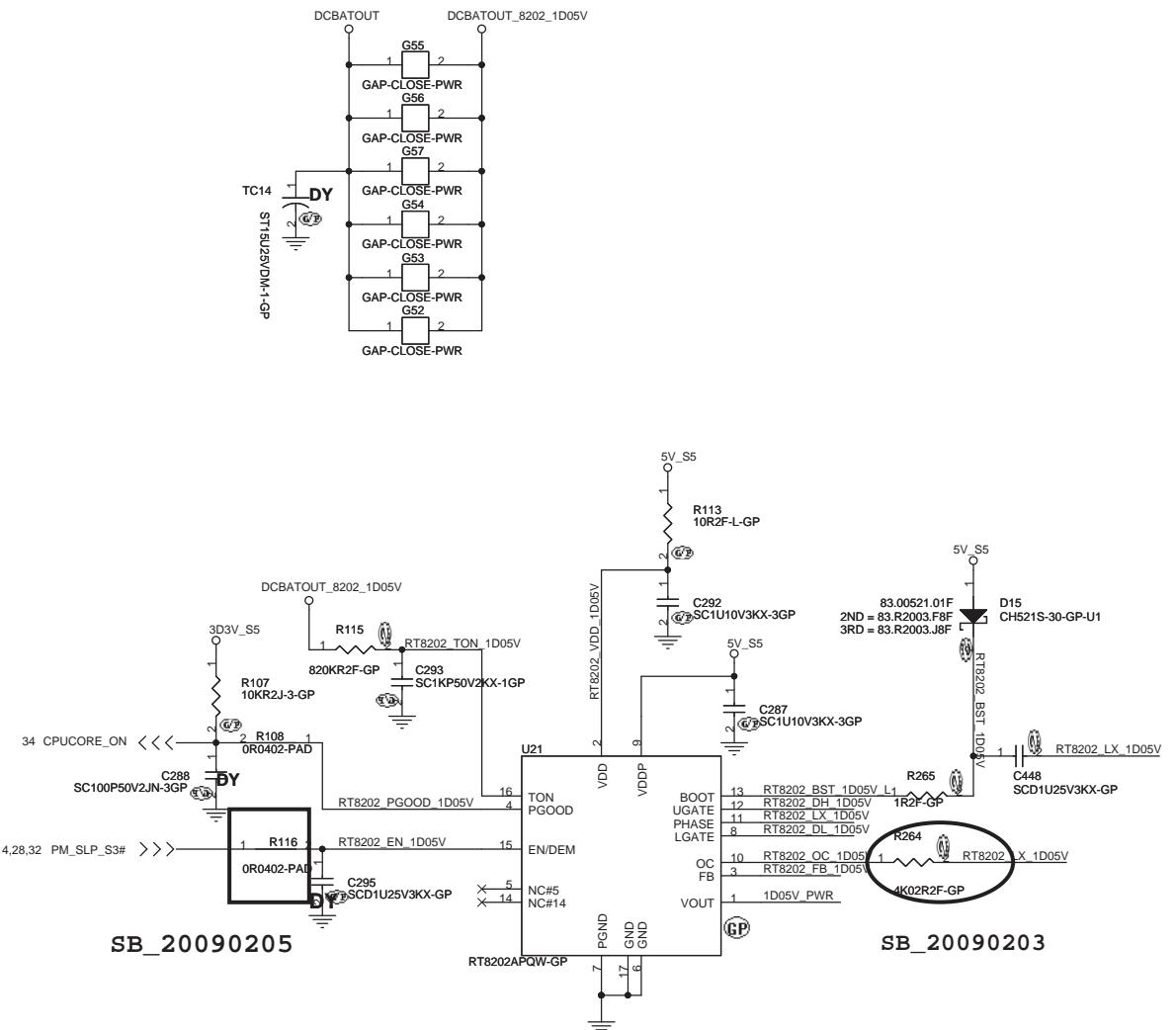
SB\_20090205

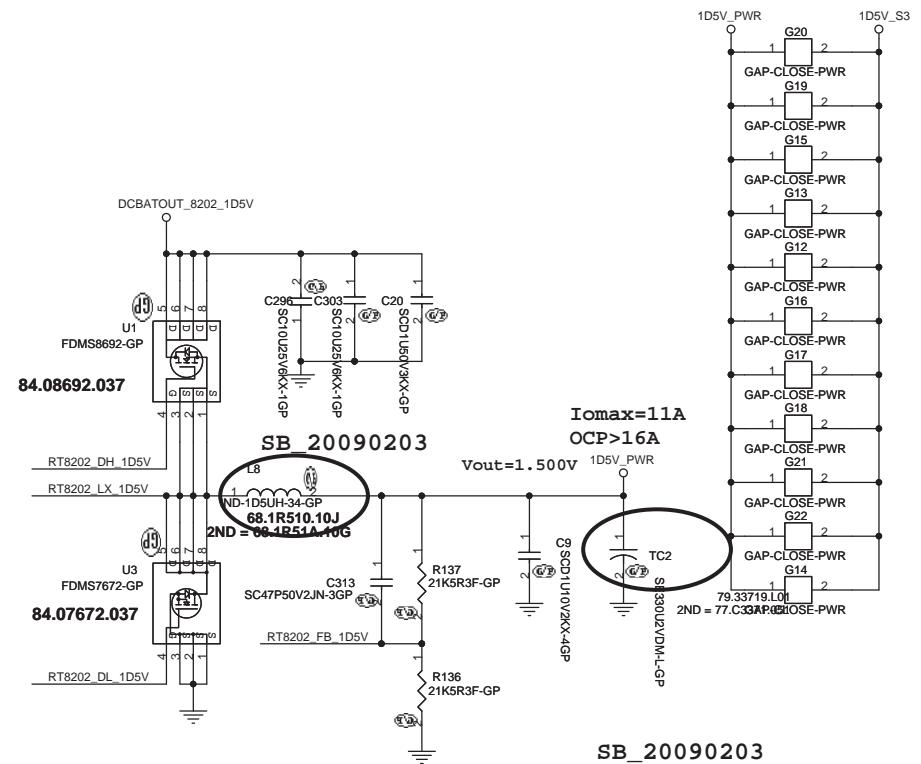
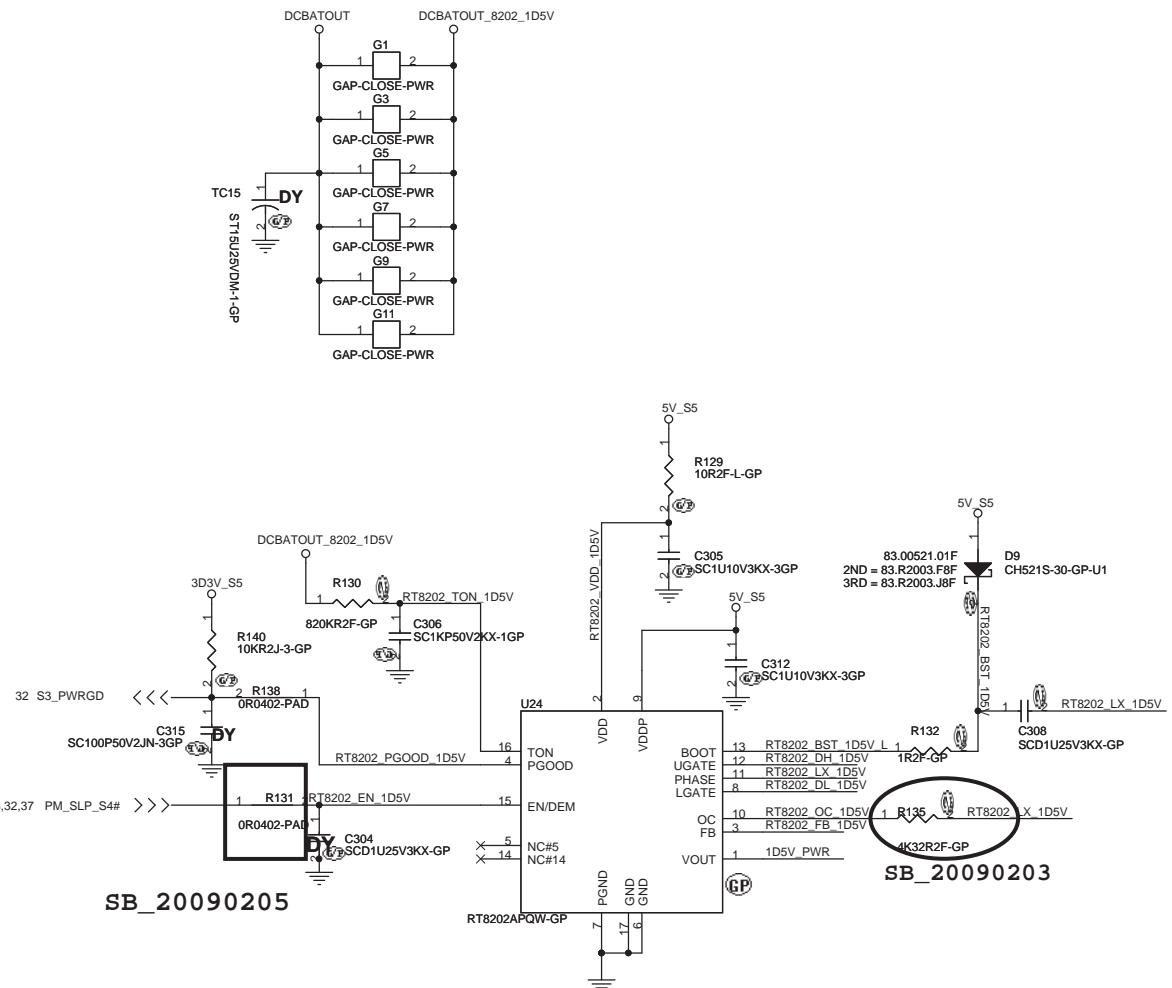


SB\_20090114



SB\_20090203





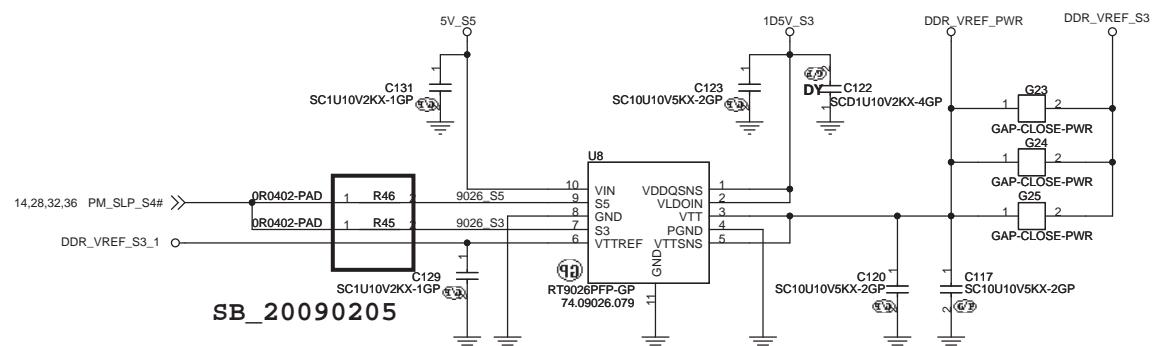
$$V_{out} = 0.75 * (1 + R_h / R_1)$$

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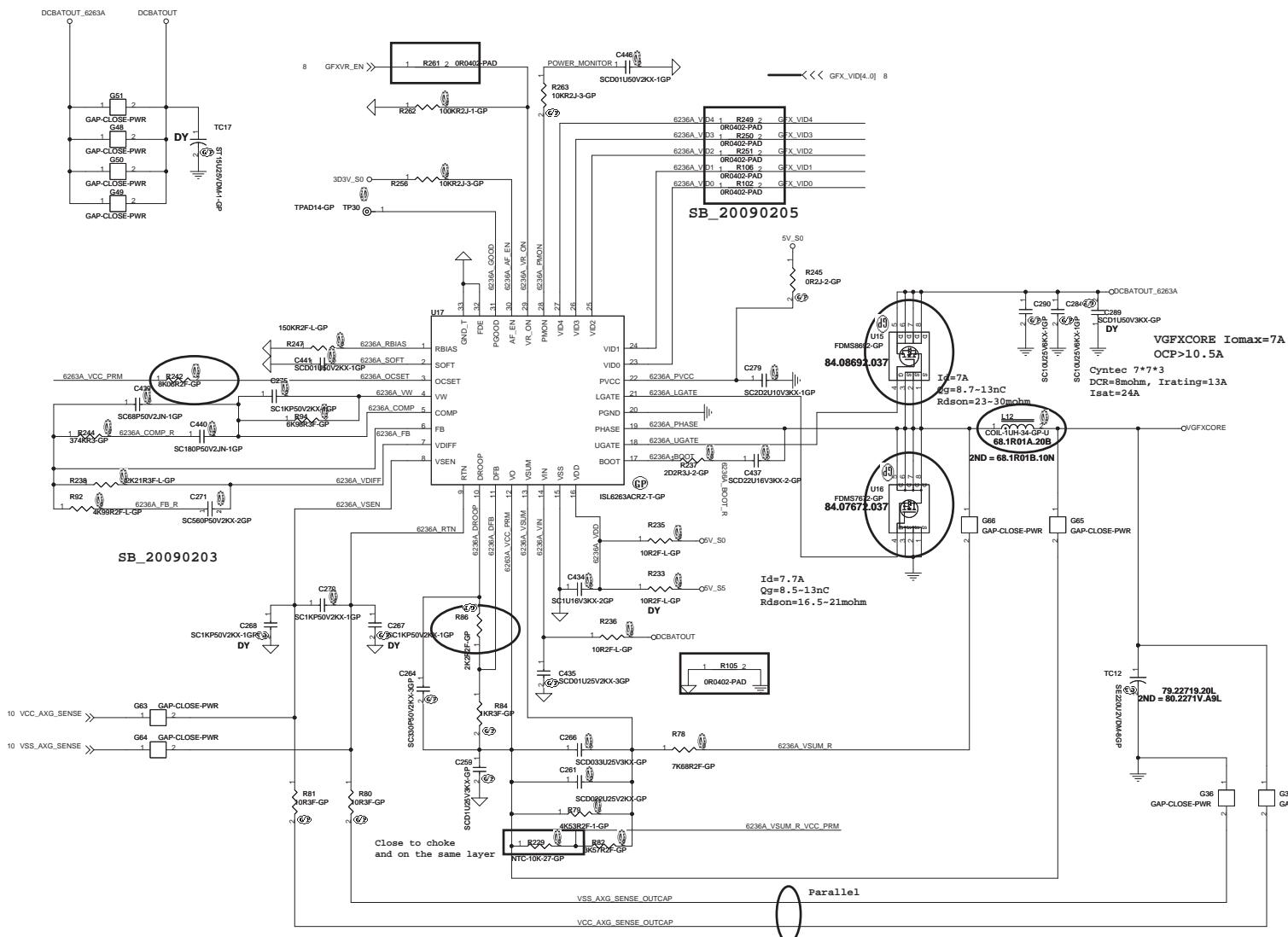
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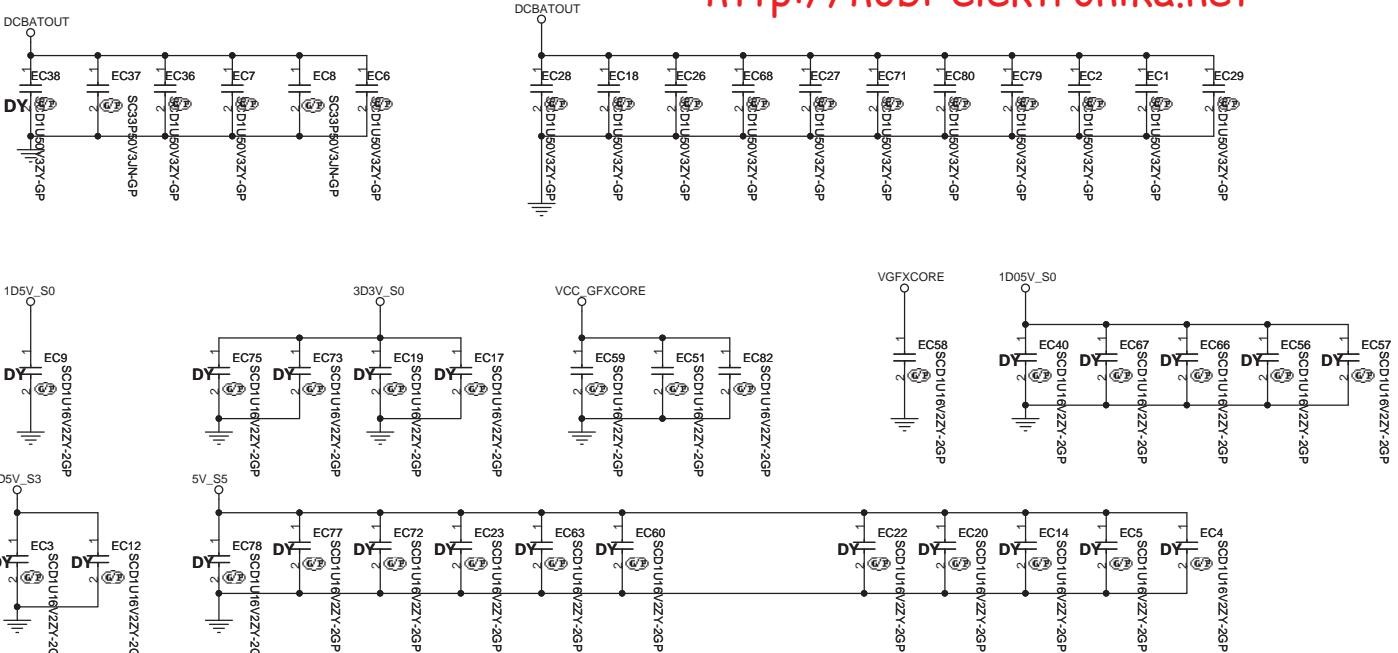
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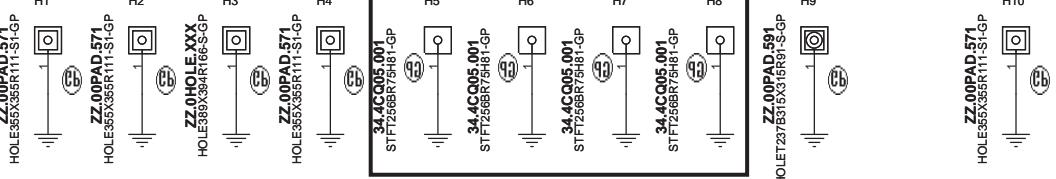
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RT9026 0D75V	
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<b>EMI/Spring/Boss</b>	
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<http://hobi-elektronika.net>

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